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CONTRACT END-ITEM
SPECIFICATION
FOR
FLEXIBLE MULTIPLEXER/DEMULTIPLEXER

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1. SCOPE

1.1 Scope This specification establishes the functional performance, design development, test, and verification requirements for the Flexible Multiplexer/Demultiplexer (FMDM).

2. APPLICABLE DOCUMENTS

2.1 Applicability The following documents of the exact issue shown shall form a part of this specification to the extent specified herein. In the event of a conflict between documents referenced herein and the contents of this specification, the contents of this specification shall take precedence.

SPECIFICATIONS

Military

MIL-I-25860B(1) 26 October 1972	Indicator, Humidity, Plug, Color Change
MIL-C-5541B(2) 30 November 1972	Chemical Conversion Coating on Aluminum and Aluminum Alloys
MIL-A-8625C(1) 13 March 1969	Anodic Coating for Aluminum and Aluminum Alloys

NASA/JSC

SP-T-0023A 10 October 1973	Environmental Acceptance Testing

Rockwell International/Space Division

MC999-0096D 30 August 1974 Amendment E-02 24 January 1975	Materials and Processes Control and Verification System for Space Shuttle Program: Suppliers and Subcontractors

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MF0004-002B 28 June 1974 Amendment C-03. 2 July 1976	Electrical Design Requirements for Electrical Equipment Utilized on the Space Shuttle Vehicle
MF0004-400 6 December 1973 Amendment A-02 25 March 1975	Electrical, Electronic, and Electro-mechanical - Orbiter Project Parts List
MF0004-100 18 October 1973 Amendment A-01 19 February 1974 Amendment A-02 5 April 1975	Mechanical - Orbiter Project Parts List
MF0004-009 5 November 1973 Amendment A-01 12 March 1974 Amendment A-02 27 March 1974 Amendment A-03 6 January 1975	Equipment Cooling Requirements, Electrical/Electronic
MC615-0010 See purchase order if any for most current issue designation	Adapter, Interface, Serial Multiplexer
MT0802-101 Rev. C dated 1-28-75	Space Shuttle Supplier Quality Program Requirements and Guidelines. Applicable requirement tables QA-M009939B, dated 4-13-75 and QA-M009939C, dated 1-13-76.
MC312-0001 Rev. C dated 1-28-75	Reliability Requirements for Suppliers and Subcontractors for the Shuttle Program, (General Requirements for). Applicable Requirements Table RA-M009939C, 4-10-75.

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MC999-0099 Rev. B dated 1-20-75	Maintainability and Support Requirements. Applicable Requirements Tables MS-M009939C, dated 4-8-75 and MS-M009939D, dated 10-02-75.
MC312-0002 Rev. B dated 1-28-75	Safety Requirements for Suppliers and Subcontractors for the Shuttle Program, (General Specification for). Applicable Requirements Table SA-M009939B, dated 4-10-75.
Rockwell Letter No. M5-153-CVH-159 dated 4-10-75	EDCP No. 1392-383-400-8 Wire Wrap
Rockwell Letter No. M5-153-CVH-158 dated 4-9-75	EDCP No. 1392-383-400-6 and 1392-383-400-7 Conductor Width and Soldering
Rockwell Letter No. M5-153-NDB-009 dated 11-27-74	Hybrid PIND Testing

Sperry

Sperry Publication No. 7104640006 dated 11-11-76	Test Verification

STANDARDS

Federal

FED-STD-101B(2) 8 October 1971	Preservation, Packaging, and Packing Materials: Test Procedures
ANSI-B46.1-1972	Surface Texture

Military

MIL-STD-12C(2) 1 February 1971	Abbreviations for Use on Drawings, Specifications, Standards and in Technical Documents

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MIL-STD-143B 12 November 1969	Standards and Specifications, Order of Precedence for the Selection of
MIL-STD-280A 7 July 1969	Definition of Item Level, Item Exchangeability Models and Related Items
MIL-STD-442(B) 1 December 1967	Aerospace Telemetry Standards
MIL-STD-129(F) 30 March 1973	Marking for Shipment and Storage
MIL-STD-130D(3) 1 August 1973	Identification Marking of U.S. Military Property
MIL-STD-794(D) (1) 25 May 1973	Parts and Equipment, Procedure for Packaging and Packing of
MIL-STD-810B(4) 21 September 1970	Environmental Test Methods
MIL-STD-1472A 15 May 1970	Human Engineering Design Criteria for Military Systems, Equipment and Facilities

OTHER PUBLICATIONS

Handbooks

DoD H 4-1 Latest Revision	Federal Supply Code of Manufacturers Name to Code
NNB6000.1(1A) December 1969	Requirements for Packaging, Handling, and Transportation for Aeronautical and Space Systems Equipment and Associated Components
ARINC Characteristics No. 568-3 Issued June 1, 1971	Airborne Distance Measuring Equipment. ARINC Aeronautical Radio Inc.

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3. REQUIREMENTS

3.1 Item Definition The FMDM shall convert and format data to provide a compatible interface between the computer complex and the subsystems. To achieve this interface, the FMDM shall (1) convert analog and discrete vehicle subsystem data to digital serial data for data bus transfer, (2) provide data buffering and format conversion between serial input/output channels, (3) convert data bus serial data into analog and discrete data for output to the vehicle subsystem. The FMDM is a "Demand-Response" system, performing its functions under control of externally supplied commands.

3.1.1 Functional Block Diagram The equipment block diagram (Figure 1) is presented for reference only. (See page 92.)

3.1.1.1 Item Description The FMDM shall consist of the following: (Duplex)

a. Two multiplexer interface adapters (MIA). (Contractor furnished equipment MC615-0010).

b. Two sequence control units (SCU).

c. Two analog-to-digital modules (A/D).

d. Up to sixteen input/output (I/O) subsystem interface modules.

e. Two power supply modules.

f. Built-In-Test Equipment (BITE) circuitry.

g. Two sequence memory modules.

The FMDM may be configured in a simplex configuration consisting of the following:

a. A multiplexer interface adapter.

b. A sequence control unit.

c. An A/D module.

d. Up to eight I/O subsystem interface modules.

e. A power supply module.

f. BITE circuitry.

g. A sequence memory module.

The FMDM to be provided in accordance with this specification shall be used to interface the payload subsystems with the vehicle computer complex. The FMDM interfaces with the data bus and payload subsystem via connectors mounted on the front panel.

For the Simplex FMDM, one connector for data bus interface and one connector for power shall be provided. For the Duplex FMDM, two connectors for data bus interface and two connectors for power shall be provided. Subsystem signal interface connectors shall be chosen to support FMDM Input/Output module interchangeability and provide for easy access (mating with ship's wiring harness connectors).

Connectors shall conform to the requirements of MF0004-002.

The FMDM shall operate under control of external signals in three modes - data transfer between Input/Output Processor (IOP), PCM Master Unit (DACBU), and FMDM; data acquisition and control between FMDM and payload subsystems; and self-test.

3.1.1.2 Unit Configuration The FMDM unit shall be capable of being configured, via the accomodation of a basic set of plug-in subsystem interface modules, to satisfy the various data acquisition and command requirements of the Orbiter vehicle. The FMDM unit shall have the capability of being configured in a redundant internal arrangement by using plug-in modules. The plug-in modules are printed circuit cards containing circuits to perform the various FMDM functions.

The design of the FMDM shall be configured so that any I/O module as defined in Paragraph 3.2.1.7 may be inserted into any of the (8) or (16) I/O connectors without causing damage to the module, and the module shall function in any of the (8) or (16) I/O connectors.

3.1.2 Interface Definition The functional and physical interface requirements between the FMDM and the interfacing subsystems are defined in the following paragraphs. The interface definition establishes the functional and physical characteristics at the interface. These require control since a change of characteristics on one side of the interface could require a design change on the other side.

3.1.2.1 Electrical Power Characteristics The electrical power characteristics at the FMDM interface shall be in accordance with MF0004-002 for main dc power as supplied over one or two independent buses; the FMDM will receive these buses on independent connectors (28 vdc).

3.1.2.2 Mechanical Interface

3.1.2.2.1 Mounting Requirements The FMDM is mounted as shown in Figures 2, 3, and 4.

3.1.2.2.2 Connector Location and Pin Function Assignments Figures 2 and 3 specify the electrical connector locations. Appendix A is a detailed connector and pin function listing.

3.1.2.3 Cooling The FMDM shall be designed for passive cooling, i.e., conduction to mounting surface and/or radiation. Thermal transfer compounds, such as silicone grease, shall not be required. For the radiation cooling mode use will be made of a suitable multilayer insulation blanket system.

The thermal radiator shall be mounted to the top of the FMDM package and, as a design goal, shall be removable, i.e., replaced with a cover plate. In this configuration, the FMDM shall be cooled via a cold plate to which the FMDM is mounted. In this case, requirements for cooling the FMDM shall be in accordance with MF0004-009 for coldplate equipment in any Orbiter location.

3.1.2.4 Signal Interface Definition The FMDM interface with the interfacing subsytems is presented in the following paragraphs.

1. FMDM To and From LRU The FMDM shall interface directly with LRUs and has the ability to provide the following signal types to the LRU.

   - Discretes (5-volts, single-ended)
     Inputs and outputs as described in Paragraphs 3.1.2.4.1.1.1.1 and 3.1.2.4.1.2.1.1.
   - Discretes (28-volts, single-ended)
     Inputs and outputs as described in Paragraphs 3.1.2.4.1.1.1.2 and 3.1.2.4.1.2.1.2.
   - DC Analog Inputs (differential and single-ended, plus 5.11 volts and minus 5.12-volts) as described in Paragraph 3.1.2.4.1.1.2.1.

- DC Analog output (plus 5.11 volts and minus 5.12 volts) as described in Paragraph 3.1.2.4.1.2.2.

- Serial I/O as described in Paragraph 3.2.1.4.

- Pulse output (28 volt) as described in Paragraph 3.1.2.4.1.2.1.3.

2. FMDM to Data Bus The FMDM shall interface directly with the digital data bus system. The data bus system provides compatible interfaces, matching isolation, fault protection, and redundance to allow the central computer system and individual FMDMs to operate as a party-line digital data transmission system. Control and monitoring, processing, and transferring of data to and from the FMDM is provided via the data bus interface. The FMDM shall interface with the data bus system using a Multiplexer Interface Adapter (MIA). The MIA shall be a functional element of the FMDM. The MIA shall function as the interface between the data bus and the FMDM control logic, receive commands and data from the data bus, and transmit response data to the data bus. The FMDM interface shall be a half-duplex channel consisting of twisted, shielded pair cables.

3.1.2.4.1 Signal Characteristics

3.1.2.4.1.1 Input Signals

3.1.2.4.1.1.1 Discrete Inputs

3.1.2.4.1.1.1.1 Discrete Input 5 Volts Discrete inputs to the FMDM at the subsystem interface shall include 5-volt, single-ended discrete input signals.

3.1.2.4.1.1.1.1.1 Electrical Characteristics The electrical characteristics of the 5-volt discrete input signals shall be as follows:

Signal Parameter	Characteristics
Digital one state (true)	Plus 5 plus or minus 1.0 volts
Digital zero state (false)	Zero plus or minus 0.5 volts

3.1.2.4.1.1.1.1.2 Discrete Input Circuits Input circuits shall be single-ended and shall be compatible with the incoming signal characteristics. The receiving circuit shall interpret an input of plus 2.0 volts or less

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difference with respect to its return line as a digital zero (false) and an input greater than plus 2.5 volts as a digital one (true). Noise suppression or filtering shall be employed for all lines driven by single-ended output circuits. The time constant of the filter employed shall be 1.0 milliseconds, plus or minus 12 percent. The signal delay resulting from the use of noise suppression of filtering circuits shall be between 0.3 and 5.0 milliseconds. Input impedance of discrete input circuits shall be between 14K ohms and 21K ohms in the digital one state and in the digital zero state. All discrete input circuits shall provide over-voltage protection of at least plus or minus 32 volts peak. The receiver shall interpret an open input line or the driver power-off impedance as specified in this document as a digital zero. The inputs shall be divided into three selectable groups (channels) with 16 inputs in each group. The input circuit shall provide no less than 10 megohms isolation between each group ground, between the FMDM internal logic ground and each group ground, and between each group ground and chassis ground.

3.1.2.4.1.1.1.1.3 Discrete Signal Return Lines Each discrete signal shall have a return line. One return for every four input discretes shall be provided and an additional three spare returns shall be provided.

3.1.2.4.1.1.1.1.4 Power-Off Impedance When de-energized, the dc impedance of the input circuit shall be no less than 10K ohms with plus or minus 6 volts or less applied.

3.1.2.4.1.1.1.2 Discrete Input 28 Volts Discrete inputs to the FMDM at the subsystems interface shall include 28-volt discrete signals.

3.1.2.4.1.1.1.2.1 Electrical Characteristics The electrical characteristics of the 28-volt discrete input signals shall be as follows:

Signal Parameter	Characteristics
Digital one state (true)	10 to 32 vdc
Digital zero state (false)	0 to 6 vdc

3.1.2.4.1.1.1.2.2 Discrete Input Circuits Input circuits shall be single-ended and shall be compatible with the incoming signal characteristics. The circuit shall interpret an input of plus 6 volts or less difference with respect to its return line as a digital zero (false) and an input greater than plus 10 volts as a digital one (true). Noise suppression or filtering shall be employed on all single-ended input circuits. The time constant of the filter employed shall be 1.0 milliseconds, plus or minus 12 percent. The signal delay

resulting from the use of noise suppression or filtering circuits shall be between 0.05 and 5.0 milliseconds. The input circuit shall provide no less than 10 megohms isolation between its input power ground return and FMDM internal logic ground. The receiving circuit shall interpret an open input line or the driver power-off impedance as a digital zero. The inputs shall be divided into three selectable groups (channels) with 16 inputs in each group. The input circuit shall provide no less than 10 megohms isolation between each group ground, between the FMDM internal logic ground and each group ground, and between each group ground and chassis ground.

3.1.2.4.1.1.1.2.3 Discrete Signal Return Lines 28-vdc discrete signal inputs shall use 28-vdc power ground. One return for every four input discretes shall be provided, plus an additional three spare returns.

3.1.2.4.1.1.1.2.4 Input Impedance The input impedance shall be between 245K ohms and 357K ohms in the logic "1" state, logic "0" state, and the power-off state.

3.1.2.4.1.1.2 DC Analog Inputs

3.1.2.4.1.1.2.1 Differential Analog inputs to the FMDM at the subsystem interface shall include differential analog signals. Prefiltering and conditioning shall be provided on these input signals to achieve common mode and passband requirements.

3.1.2.4.1.1.2.1.1 Electrical Characteristics The electrical characteristics of the input signals shall be as follows:

- Signal Type Differential or single-ended.
- Full Scale Voltage Range From plus 5.11 volts to minus 5.12 volts.
- Source Impedance 100 ohms maximum with a maximum unbalance of 10 ohms for differential inputs. For single-ended inputs, the source impedance shall be 100 ohms maximum.

3.1.2.4.1.1.2.1.2 Input Circuit Characteristics The input characteristics of the FMDM for differential analog input signals shall be as follows:

- Input Impedance

  500 Kilohms minimum during sampling
  500 Kilohms minimum during non-sampling
  100 Kilohms minimum when FMDM power is off

- Common Mode Rejection 60 dB within the passband (as specified by Paragraph 3.1.2.4.1.1.2.1.3c) for common mode signals between plus and minus 10-volt minimum amplitudes for all signal ranges.

- Signal Lead Termination High and low input pins shall be provided for each differential analog input signal on the FMDM signal input connector.

3.1.2.4.1.1.2.1.3 Signal Processing Characteristics FMDM signal processing characteristics shall be as follows:

a. Encoding Accuracy The analog signals shall be sampled and encoded by the FMDM for transmission onto the data bus. The total accumulated end-to-end errors contributed by the FMDM to the input signal due to any internal error source or any combination of environment, power-source voltage, and signal-source impedances specified herein shall not exceed 0.5 percent RMS of the full-scale voltage. The following error model is provided for analytical use:

Parameter	Description	End of Life (one sigma)
Scale factor	Gain error in A/D or D/A processing	±0.40% of input value
Bias	Circuit null offset errors in A/D or D/A processing	±0.20% full scale
Noise	Circuit-noise-induced errors in A/D or D/A processing. (Noise is assumed band limited white to 10K Hz)	±0.20% of full scale
Quantization	A/D encoding nonlinearity or D/A decoding nonlinearity	±0.10% of full scale

The maximum end-of-life value can be taken as the two-sigma value for 95 percent confidence and three sigma for 99 percent confidence.

b. Open Circuit Encoding An open input circuit shall be encoded by the FMDM to an "all zeros" code plus or minus the binary equivalent of 25 millivolts. An open input circuit is defined as a source impedance greater than 10 megohms.

c. Pre-Sample Filter The pre-sample filter shall be a low-pass filter whose 3-dB point is at 40 Hz, plus or minus 10 percent, and roll-off thereafter at a minimum rate of 6 dB per octave. The design shall provide for ease of alternation of the passband characteristics. The input filter shall be implemented to be bypassed by the user.

3.1.2.4.1.1.3 Serial Digital The serial digital input interface is defined in Paragraph 3.2.1.4.

3.1.2.4.1.2 Output Signals

3.1.2.4.1.2.1 Discrete Outputs

3.1.2.4.1.2.1.1 Discrete Output 5 Volts Discrete outputs from the FMDM at the payload subsystem interface shall include 5-volt discrete signals.

3.1.2.4.1.2.1.1.1. Electrical Characteristics The electrical characteristics of 5-vdc discrete outputs shall be as follows:

Signal Parameters	Characteristics
Digital one state (true)	Plus 5 plus or minus 1.0 volts
Digital zero state (false)	Zero plus or minus 0.5 volts
Rise Time*	1.0 to 20.0 microseconds
Fall Time*	1.0 to 20.0 microseconds

*The rise and fall time shall be measured between 10 and 90 percent of the peak signal limits driving a resistive load of 400 ohms, plus or minus 5 percent, paralleled with 5000 picofarads, plus or minus 10 percent.

3.1.2.4.1.2.1.1.2 Discrete Output Circuit The single-ended discrete outputs shall be capable or supplying 10 milliamperes current at plus 4.0 volts minimum. The output circuit shall be capable of driving no less than 50 feet of single-conductor cable having a distributed capacitance of 50 picofarads per foot, with no less than four input circuits on the line, each drawing 1.25 milliamperes maximum. The output circuit shall be capable of sinking 10 milliamperes of current when at 0.5 volts.

3.1.2.4.1.2.1.1.3 Power-Off Impedance When de-energized, the dc impedance of the output circuit shall be no less than 10K ohms with plus 6 volts applied.

3.1.2.4.1.2.1.1.4 Signal Ground The FMDM 5-volts dc output module shall provide 16 signal grounds. One ground for every four output discretes and an additional four spares shall be provided.

3.1.2.4.1.2.1.2 Discrete Output 28 Volts Discrete output from the FMDM at the vehicle subsystem interface shall be 28 volts dc nominal, and in accordance with MF0004-002.

3.1.2.4.1.2.1.2.1 Electrical Characteristics The electrical characteristics of 28-volts dc discrete outputs shall be as follows:

Signal Parameters	Characteristics
Digital one state (true)	Vehicle power-voltage level with allowable 4.5 volts internal voltage drop
Digital zero state (false)	0 to 3 vdc maximum
Rise Time*	10.0 microseconds to 100.0 microseconds
Fall Time*	10.0 microseconds to 100.0 microseconds

*The rise and fall time shall be measured between 10 and 90 percent of the peak signal 28-volt limits, driving a resistive load of 2.8K ohms, plus or minus 5 percent, paralleled with 5000 picofarads, plus or minus 10 percent.

3.1.2.4.1.2.1.2.2 Discrete Output Circuit The single-ended discrete outputs shall be capable of supplying 10 milliampere current maximum at plus 18 volts dc. The output circuitry shall be an electronic switch for obtaining a

discrete output signal by utilizing 28 volts dc vehicle power. The power ground isolation from the internal FMDM signal ground shall be provided with a minimum of 10 megohm isolation capability for each discrete output.

3.1.2.4.1.2.1.2.3 Power-Off Impedance When de-energized, the dc impedance of the 28 volts dc discrete output shall be no less than 10K ohms, with plus 8 volts input applied.

3.1.2.4.1.2.1.2.4 Signal Ground The vehicle power ground shall be utilized for the 28 volts dc discrete outputs. The FMDM 28-volt dc output module shall provide 16 signal grounds. One ground for every four output discretes and an additional four spares shall be provided.

3.1.2.4.1.2.1.3 Pulse Output 28 Volts Pulsed outputs from the FMDM at the payload subsystem interface shall be 28 volts peak nominal and in accordance with MF0004-002.

3.1.2.4.1.2.1.3.1 Electrical Characteristics The electrical characteristics of 28-volts dc discrete outputs shall be as follows:

Signal Parameters	Characteristics
Positive Pulse Level (true)	Vehicle power-voltage level with allowable 4.5 volts internal voltage drop
Zero Level (false)	0 to 3 volts dc maximum
Rise Time*	10.0 microseconds to 100.0 microseconds
Fall Time*	10.0 microseconds to 100.0 microseconds
Pulse Width	20 milliseconds minimum, 35 milliseconds maximum
Duty Cycle	20% maximum duty cycle; the maximum number of outputs which can be in the true state at any one time is 24

*The rise and fall time shall be measured between 10 and 90 percent of the peak signal 28-volt limits, driving a resistive load of 580 ohms (plus or minus 5 percent) paralleled with 5000 picofarads, plus or minus 10 percent.

3.1.2.4.1.2.1.3.2 Pulse Output Circuit The single-ended discrete outputs shall be capable of supplying 50 milliampere current maximum at plus 18 volts. The output circuitry shall be an electronic switch for obtaining a discrete output signal by utilizing 28-volts dc vehicle power. The power ground isolation from the internal FMDM signal ground shall be provided with a minimum of 10 megohm isolation capability for each discrete output.

3.1.2.4.1.2.1.3.3 Power-Off Impedance When de-energized, the dc impedance of the 28-volt dc pulse output shall be no less than 10K ohms, with plus 8 volts input applied.

3.1.2.4.1.2.1.3.4 Signal Ground The vehicle power ground shall be utilized for the 28-volt dc pulse outputs. The FMDM 28-volt dc output module shall provide 16 signal grounds which includes one ground for every four output discretes and an additional four spares.

3.1.2.4.1.2.2 DC Analog Outputs

3.1.2.4.1.2.2.1 Differential Outputs The output circuit shall be differential, and shall exhibit a maximum output impedance of less than 100 ohms, with a maximum unbalance of 10 ohms. The output circuit shall be capable of supplying 8 milliamperes minimum at plus 5.11 volts, and sinking 8 milliamperes at minus 5.12 volts. The output circuit shall be capable of driving no less than 50 feet of two-conductor cable with a distributed capacitance of 50 picofarads per foot. DC output voltage range shall be plus 5.11 volts to minus 5.12 volts. The output circuits shall not be damaged or shall not malfunction if shorted to ground for an indefinite period of time, or if plus or minus 32 volts are applied line to ground. When one output amplifier is shorted to ground, however, the remaining output can only sink 1.25 mA and source 2.5 mA. The product of this current and the subsystem device resistance determines the maximum voltage swing in the presence of a short circuit. The output circuit shall be limited to plus or minus 15-volt output maximum. Channel accuracy shall be 0.5 percent rms full scale; output sample and hold circuits shall exhibit less than 0.1 percent droop over a 100-millisecond time period. The dc output circuit shall be capable of accomplishing full-scale voltage slew in less than 30 microseconds. See Paragraph 3.1.2.4.1.1.2.1.3a for an error model for analytical use.

3.1.2.4.1.2.2.2 Power-Off Impedance When de-energized, the dc output impedance shall be no less than 10K ohms, with plus 8 volts input applied.

3.1.2.5 Data Bus The FMDM design shall incorporate a MIA as defined in MC615-0010.

3.1.2.5.1 MIA/FMDM Interface

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3.1.2.5.1.1 Electrical Design The FMDM design shall be compatible with the MIA/Host Interface and timing defined in MC615-0010.

3.1.2.5.1.2 Electrical Power The FMDM design shall provide electrical power to the MIA as defined in MC615-0010.

3.1.2.5.1.3 Heat Dissipation The FMDM design shall provide for MIA heat dissipation as defined in MC615-0010 except that the heat-sink temperature range shall not exceed 196°F and the thermal resistance between MIA and heat sink shall not exceed 1.26°F per watt.

3.1.2.5.1.4 Mechanical Design The MIA shall be installed in accordance with the mounting provisions as defined in MC615-0010. The MIA shall not be subjected to vibration levels in excess of the envelope listed below:

20 -	80 Hz	- Rising at 3.2 dB/octave from 0.08 to 0.35 g^2/Hz
80 -	140 Hz	- Constant at 0.35 g^2/Hz
140 -	350 Hz	- Rising at 12.8 dB/octave from 0.35 to 14.0 g^2/Hz
350 -	500 Hz	- Falling at 11.8 dB/octave from 14.0 to 2.0 g^2/Hz
500 -	1000 Hz	- Constant at 2.0 g^2/Hz
1000 -	2000 Hz	- Falling at 18.2 dB/octave from 2.0 to 0.03 g^2/Hz

3.1.2.5.1.5 Data Bus Interconnection Unless otherwise approved by the buyer, the interface cable from the FMDM LRU connectors to the MIA data bus pin connections shall be two-conductor, twisted, shielded, jacketed cable with a distributed capacitance of less than 50 pf per foot, and an impedance of 70 ohms, plus or minus 10 percent.

3.1.2.5.1.6 MIA Address Decoding The FMDM shall provide independent MIA address coding for each MIA within the FMDM. The connector(s) containing the data bus interface wiring shall contain at least seven pins to permit setting the MIA address externally in the wire harness. The FMDM (SCU module) shall decode the MIA address by the use of five of these pins which shall provide access to the FMDM logic circuitry for Bits 4 through 8 of the Command/Command Data Words, a sixth pin which shall provide a logic one voltage source, and a seventh pin for a logic zero voltage source. The MIA address for the FMDM shall be established by the wire harness connections, and shall be generated within the FMDM for response data word encoding. The MIA address established by the wire harness connection shall not be wired externally to accept a MIA address of zero.

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3.1.2.5.2 Data Bus Transfer Methods

3.1.2.5.2.1 Modulation The modulation shall be in accordance with MC615-0010.

3.1.2.5.2.2 Data Code The data code shall be in accordance with MC615-0010.

3.1.2.5.2.3 Data Rate The data rate shall be in accordance with MC615-0010.

3.1.2.5.2.4 Message The message shall be in accordance with MC615-0010.

3.1.2.5.2.5 Command Word Sync . The command word sync shall be in accordance with MC615-0010.

3.1.2.5.2.6 Data Word Sync The data word sync shall be in accordance with MC615-0010.

3.1.2.5.2.7 Transmission Line The transmission line shall be in accordance with MC615-0010.

3.1.2.5.3 Output Circuit Characteristics

3.1.2.5.3.1 Output Circuit Voltage The output circuit voltage shall be in accordance with MC615-0010.

3.1.2.5.3.2 Output Waveform The output waveform shall be in accordance with MC615-0010.

3.1.2.5.3.3 Transmitter Output Noise The transmitter output noise shall be in accordance with MC615-0010.

3.1.2.5.3.4 Transmitter Off Impedance The transmitter off impedance shall be in accordance with MC615-0010.

3.1.2.5.3.5 Output Waveform Distortion The output waveform distortion shall be in accordance with MC615-0010.

3.1.2.5.4 Input Circuit Characteristics

3.1.2.5.4.1 Input Circuit Common Mode Rejection The input circuit characteristics shall be in accordance with MC615-0010.

3.1.2.5.4.2 Input Circuit Impedance The input circuit impedance shall be in accordance with MC615-0010.

3.1.2.5.5 Gap Time The FMDM shall be responsible for defining the gap time between successive data transmissions as defined in MC615-0010. The gap time shall be controlled by the leading edge of the Transmit Data Available pulse.

3.1.3 End Item and Major Component Identification The identification of the multiplexer/demultiplexer unit shall be as specified in Appendix A.

3.1.4 Buyer Furnished Property The following items will be supplied by the buyer, and shall be incorporated into the FMDM.

Nomenclature	Buyer Control/Part No.	Traceability Classification	Maintenance Level
Adapter, Interface, Serial Multiplexer	MC615-0010-0XXX*	Serial	SRU

*The current dash number will be supplied by purchase order change notice.

3.2 Characteristics

3.2.1 Performance The FMDM shall be capable of sampling analog, discrete, and serial digital signals from the vehicle subsystems on command from the vehicle computers. The FMDM shall also be able to output dc analog signals, discrete signals, and serial digital signals to the payload subsystems.

3.2.1.1 Life Requirements The FMDM shall be designed to provide the most cost-effective life capability, considering minimum maintenance and refurbishment as well as state-of-the-art hardware design.

3.2.1.1.1 Operating Life As a design objective, the FMDM shall be capable of performing all operations specified herein for a minimum of 24,000 hours.

3.2.1.1.2 Useful Life As a design objective, the MDM shall have a minimum useful life of 24,000 hours, which is equivalent to 100 orbital missions in a 10-year period from date of delivery. The average orbital mission will be seven days; however, the design shall not preclude the capability to extend the orbital staytime up to 30 days. Preventive maintenance, servicing, repair, and replacement of parts shall be consistent with the seller's tradeoff results, as agreed to by the buyer.

3.2.1.1.3 Shelf Life As a design objective, the FMDM shall be capable of operating in accordance with the requirements specified herein any time within a period of 10 years from date of delivery when exposed to the applicable environments of 3.2.5.

3.2.1.2 Functional Requirements

3.2.1.2.1 Functional Arrangement The simplex FMDM shall be packaged in a single box. Space and connectors shall be provided in the FMDM box for a total of eight I/O modules, each with a maximum of 32 addressable I/O channels. The I/O modules shall be of nine types for initial configuration, as defined by this document. Any number of I/O modules (eight maximum) in any configuration mix may be inserted into the FMDM to accommodate vehicle interface requirements for data acquisition and control. An I/O channel may be 16 single-ended discrete signals plus ground, a serial I/O channel, or other. The design of the FMDM modules shall be compatible with duplex configurations or other expanded simplex arrangements employing any number of I/O modules in any configuration mix up to 16 I/O modules maximum.

3.2.1.2.2 Power Supplies The FMDM shall contain power supplies which convert input dc power to required internal operating voltages. Operation of the power supplies shall be coordinated and sequence-controlled during turn-on and turn-off, input power interruption and transients to assure a predictable initial operating state and continuity of operation. Application and removal of input power shall be sensed; power-off and power-on interrupt signals generated, and internal protective operation conducted as required to provide the response specified herein. Should one supply shut down, the other power supply shall assume the FMDM power load and the FMDM operation shall not be affected (i.e., a Duplex FMDM).

Current limiting of the 28-volt external power and diode OR-ing on the 28-volt output discrete modules shall be used. Diode OR-ing of the 28-volt external power within the FMDM shall not be used except for the 28-volt discrete output modules.

3.2.1.2.3 Power-On Sequence Application of input power to the FMDM shall be sensed, and shall initiate an orderly start-up sequence and an orderly initialization sequence that contains steps in this order:

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a. Sense input power application.

b. Reset all FMDM outputs to logic "0". Discrete outputs may be indeterminate for a period not to exceed 200 microseconds, after which discrete outputs shall be at a logic "0" state.

c. Inhibit all outputs from changing state for 10 milliseconds.

d. Set Bit 1 of the internal BITE status register to a logic "1".

e. Set all remaining BITE bits to logic "0".

f. Begin normal FMDM operation 10 milliseconds after input power is sensed.

The S-bit shall be set to "0" on the first response data word transmitted by the FMDM following a power-down/power-up sequence which normalized FMDM registers. The S-bit shall be reset to "1" by the first word of the next data message. If the first word transmitted following a power transient is BITE status, the "S" indication shall not be given in the SEV field of the response data word.

Bit 1 shall be set in each BITE status register following the occurrence of a power-down/power-up sequence which normalized FMDM outputs. The indication shall remain in the BITE status register until reset following GPC BITE status request or by GPC commanded master reset.

3.2.1.2.4 Power-Off Sequence Removal of both external power input sources from the FMDM shall be sensed, and shall initiate an orderly power shutdown sequence containing, but not limited to, the following steps:

a. Sense power removal at the input power filter and generate a power-down reset function when the voltage has reached a level below which normal operation cannot be maintained. (Capacitive energy storage shall sustain operation as required for power interruption holdover, as per Paragraph 3.2.1.2.5).

b. Complete orderly shutdown by setting all discrete outputs to a logical zero within 250 microseconds. Following power-down reset of the analog output module, the output differential voltage shall

not exceed 320 millivolts peak for loads no greater than 500K ohms, line to line, and either line to ground voltage shall not exceed 1000 millivolts peak for loads no greater than 1 megohms line to ground. The output differential voltage shall remain less than 25 millivolts peak subsequent to 100 milliseconds following power-down reset.

c. Complete orderly shutdown by setting all external interfaces to logic "0".

Once shutdown starts, the sequence shall continue to completion regardless of subsequent input power status.

3.2.1.2.5 Power Interruption Starting from an input of 28 vdc, loss of input power for periods of up to two milliseconds at +25°C shall not affect FMDM operation. At -55°C, loss of input power for up to one millisecond shall not affect FMDM operation. The FMDM is not required to operate if loss of input power exceeds two milliseconds.

3.2.1.2.6 Normal Power Transients Input power transients within the limits defined in Specification MF0004-002 shall not cause FMDM malfunction or affect FMDM operation.

3.2.1.2.7 Abnormal Power Transients Input power transients within the limits defined in Specification MF0004-002 shall not cause equipment damage or spurious behavior. For undervoltage transients which exceed normal limits, execution of a shutdown/restart sequence is permissible provided all the sequence steps of Paragraphs 3.2.1.2.3 and 3.2.1.2.4 are executed.

3.2.1.2.8 Electrical Protection (Internal) Protection shall be provided in the FMDM where a failure, fault, or overload could result in the following:

- Chain reaction failure causing loss or failure of other major components.
- Significant hazards of fire, smoke, or explosion.
- Damage of external wiring or output circuits.

Circuit breakers, fuses, or similar devices shall not be used. Only automatically resetting elements that sense such FMDM internal characteristics as overcurrent, overvoltage, or overtemperature shall be utilized.

3.2.1.3 SCU Functions The Duplex FMDM SCU serves as a central control element for each of two functional areas (see Figure 1) that are defined as follows:

- Functional area 1 - consists of MIA 1, SCU 1, A/D 1, data/address channel 1, any of the I/O modules, and the power supply. SCU 1 controls the operation of this FMDM area.
- FMDM functional area 2 - consists of MIA 2, SCU 2, A/D 2, data/address channel 2, any of the 16 I/O modules, and the power supply. SCU 2 controls the operation of this FMDM area. The addressing of FMDMs on the primary and backup data buses at the same time is an error condition, and the FMDM shall not respond.

The major SCU functions shall be as follows:

- Accept data from the MIA.
- Decode FMDM address, I/O module address, and mode field to determine the required operational mode. Execute the specified mode of operation.
- Enable addressed I/O modules.
- Transmit channel address and data to I/O modules.
- Control operation of the A/D converter.
- Provide for transfer of command data word (CDW) to the I/O modules at the same time as the incoming message parity and validity is being verified.
- Accept data from I/O modules.
- Establish response data word format and transmit the data to the MIA.
- Perform self-test to determine FMDM operational status.
- Set a bit in the BITE status register to a logical "1" when an external device requests an operation on a nonexistent channel. The operation shall not be executed.

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- The SCU shall assign addresses 1 through 31 to the FMDM. Address selection shall be accomplished as described in Paragraph 3.1.2.5.1.6.

- Data bus interword gap-time shall be monitored in the FMDM; incoming data gap-time shall be 5.5 plus and minus 0.5 microseconds (Reference Figure 9).

The FMDM interword gap-time, sync included, may be checked at any time between 11 and 38 microseconds. The time checked shall be from the end of a word to the start of the next word within the message. Failure to meet the gap-time requirement shall set Bit 10 in the BITE status register.

- The SCU shall detect simultaneous operation from the primary and backup data bus and set Bit 7 in the BITE status register when an error condition exists. The SCU shall discontinue all operations until a new command data word is received.

- Data bus interword gap time for words transmitted from the FMDM shall be 5.5, plus or minus 0.5 microseconds (Reference Figure 10).

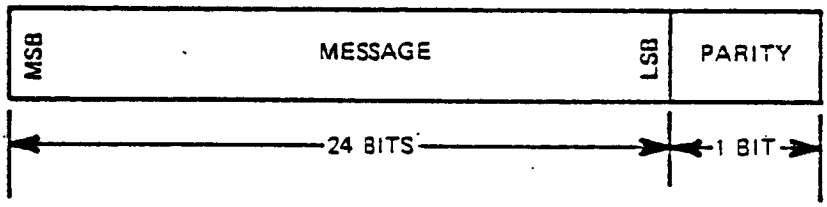
- The SCU shall verify the Command Data Word (CDW) check pattern consisting of Bits 25 through 27, (101). Command data words failing the 101 check shall be considered bad data words, and shall be treated in accordance with Paragraph 3.2.1.3.2.1.

3.2.1.3.1 Word Size The word size shall be 24 bits, plus sync, plus parity, as shown in Figures 7 and 8.

3.2.1.3.1.1 Word Format The word format (bit definition) shall be as shown in Figures 7 and 8.

3.2.1.3.1.2 Number of Words The number of words in a message shall be from 1 to 33 maximum for data bus commands. Where data bus command words specify use of the PROM, the number of words in a message can be up to a maximum of 512 data words (32 PROM locations times 16 words).

3.2.1.3.1.3 Parity Bit Each word shall contain a parity bit. During transmission the parity bit shall be assigned a value so the total number of "ones" in the word is odd. During reception, the parity shall be checked by determining whether or not the received word contains an odd number of ones; Bits 4 through 28 must be odd.



3.2.1.3.2 Message Format The message format shall be as specified by this document. The format of the command and data words (bit designation) shall be as shown in Figures 7 and 8.

3.2.1.3.2.1 Message Sequence The FMDM shall be capable of satisfying the peak through-put requirements of half duplex data bus in that it shall accept data bus Command Words (CW) or Command Data Words (CDW) at a peak rate of one each 28 microseconds, plus gap time plus or minus 0.5 microsecond, or output Response Data Words at a peak rate of one each 28.0 plus or minus 0.5 microsecond plus gap time.

a. The message sequence for the transfer of data to an FMDM shall consist of the following form (See Figure 9):

- One command word followed by 1 to 32 data words from the data bus.

- If a command word is not accepted by FMDM, the FMDM shall not respond to the subsequent command data words in that message. If a bad command data word is received, subsequent command data words of the message will not be accepted by the FMDM. The FMDM shall set a Bit 2 in the BITE status register and wait for a new command word.

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b. The message sequence for data requested from an FMDM shall consist of the following form (See Figure 10).

- One command word from the data bus followed by 1 to 32 response data words transmitted by FMDM.
- If a command word is not accepted by the FMDM, the FMDM shall not transmit a response word.

3.2.1.3.2.2 Command Word The command word shall contain the following information:

Bits

1-3 Command Sync - Three-bit nonvalid Manchester code as defined by this document.

4-8 FMDM Address - Five-bit code that identifies the FMDM that shall respond to a given command. Addresses shall be assigned from 1 to 31. Address zero (00) shall not be assigned as an FMDM address.

9 Spare

10-13 Mode Control Field - Four-bit code used for determining the operational mode of the FMDM.

14-17 Module Address - Four-bit code that identifies the I/O module where the selected channels are located. All zeros coded in Bits 14-17 addresses module address one; all ones address module 16.

18-22 Channel Address - Five-bit code that identifies one out of a maximum of 32 channels on the I/O module. This code also identifies a starting channel address for a multiple-word data transfer. Refer to Figure 7 for unique use of these bits for discrete outputs.

All zeros coded in Bits 18-22 addresses channel address one; all ones addresses channel address 32.

23-27 Number of Words - Five-bit code that identifies the number of data words to be transmitted or received. For a nonzero code, the FMDM shall transmit/receive words from/to a channel address increasing monotonically starting from the channel address Bits 18 through 22.

If an addressed module contains 32 channels, the channel address can wrap around on the module. Channel addressing shall not increase monotonically to the next higher module address.

28 Parity - Odd parity as defined by this document.

3.2.1.3.2.3 Command Data Word The command data word shall contain the following information:

Bits

1-3 Data Sync - Three-bit nonvalid Manchester code for a command data sync as defined by this specification.

4-8 FMDM Address - Five-bit code that identifies the FMDM that shall respond to a given command. Addresses shall be assigned from 1 to 31. Address zero shall not be assigned as an FMDM address.

9-24 Data - Contains the data to be transferred from the GPC to the subsystem.

25-27 FMDM Pattern Code - FMDM pattern code for message validity test.

28 Parity - Odd parity as defined by this document.

3.2.1.3.2.4 Response Data Word The response data word shall contain the following information:

Bits

1-3 Data Sync - Three-bit nonvalid Manchester code for a response data sync as defined by this specification.

4-8 FMDM Address - Five-bit code that identifies the FMDM responding to the command word.

9-24 Data - Contains the requested subsystem or BITE data.

25 S-Bit Power Transient Indication - The S-bit shall be set to "0" on the first response data word transmitted by the FMDM following a power-down/power-up sequence which normalized FMDM registers. The

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S-bit shall be reset to "1" by the first word of the next data message. If the first word transmitted following a power transient is BITE status, the "S" indication shall not be given in the SEV field of the response data word.

Bit 1 shall be set in each BITE status register following the occurrence of a power-down/power-up sequence which normalized FMDM outputs. The indication shall remain in the BITE status register until reset following GPC BITE status request or by GPC commanded master reset.

26 E-BIT Subsystem Serial Channel Error Flag - The E-bit shall be set to "1" on response data words for which a handoff error has been detected when transferred to the FMDM over a subsystem serial channel. The E-bit shall indicate any serial channel handoff error which the FMDM is mechanized to detect (such as parity, invalid Manchester bit count, no response, or missing word). The FMDM shall return at least one data word with the E-bit set to "1" following a no-response or data word dropout. The FMDM shall indicate E-bit errors only within the message for which an error was detected. Errors indicated with the E-bit shall not be indicated in the BITE status register.

27 V-BIT Data Validity - The V-bit shall be used to indicate FMDM failures which cause the data in the current transmission to be suspect. The V-bit shall be set to "0" on data words for which an internal FMDM failure (that may affect current data validity) occurred during processing of that data. The V-bit shall be reset to "1" by the first word of the next data message. Failures that do not affect validity of data transmitted on the data bus shall be indicated in the BITE register, but shall not cause the V-bit to be set to "0". Errors detected in commands and data received on the data bus by the FMDM shall be indicated in the status register, but shall not cause the V-bit to be set to "0" on any subsequent response data words.

28 Parity - Odd parity as defined by this specification.

3.2.1.3.2.5 Message Intervals The message intervals shall conform to Figures 9 and 10.

3.2.1.3.2.6 Failure of FMDM to Access I/O Interface Modules If for any reason the FMDM is unable to transfer received data from the subsystem I/O modules, Bit 4 of the BITE status register shall be set and the validity bit (Bit 27) of the response data word shall be set invalid, on a word-by-word basis.

3.2.1.4 Serial Digital I/O Channel The characteristics of serial-digital input/output channels between FMDM and the vehicle subsystem shall be half-duplex, Manchester II bi-phase, at a 1-megabit rate.

3.2.1.4.1 Channel Interface One serial-digital I/O channel shall consist of the following: (See Figure 11.)

- Data
- Word discrete output
- Message-out discrete output
- Message-in discrete output

In Orbiter operation, some channels or message lines within a channel may not be connected to an external subsystem.

3.2.1.4.2 Cable The cable used to transfer serial-digital data and enable signals shall be a two-conductor, twisted, single-shield, jacketed cable equivalent to a twin-axial cable having 71 ohms, plus or minus 10-percent impedance, with a distributed capacitance no greater than 50 picofarads per foot. There shall be one cable dedicated to the transmission of data words, one cable dedicated to message-in enable, one cable dedicated to message-out enable, and one cable dedicated to word discrete.

3.2.1.4.3 Input/Output Circuit Characteristics The message-in discrete, message-out discrete, word discrete (Figure 12) shall be differential (double-ended) monotonically, changing discrete outputs. The output circuit shall be capable of driving no less than 150 feet of cable (see Paragraph 3.2.1.4.2). The discrete output circuits shall be electrically referenced to the FMDM signal ground. Skew between signal outputs of the differential driver shall not exceed 50 nanoseconds. Plus or minus 32 volts applied through 320 ohms to any message or word discrete output line shall not cause FMDM

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malfunction or affect FMDM operation. This overvoltage shall only appear on one line at a time. The electrical characteristics of discrete output signals shall be as follows:

Signal Parameter	Characteristics
Type	Differential output
Logic Level "one"	Plus 3.0 to 5.0 volts
Logic Level "zero"	Minus 3.0 to minus 5.0 volts
Output Impedance - line-to-line or line-to-ground	50 ohms (maximum) over the frequency range of 500 KHz to 3.5 mHz and 100 ohms maximum from dc to 10 KHz
Overshoot and Undershoot	0.25 volts (maximum)
Load Impedance (L/L)	
Cable less than 50 feet or	75 ohms plus or minus 10 percent in series with 0.0033 mfd plus or minus 10 percent
Cable less than 150 feet	90 ohms, plus or minus 5%, in series with 0.01 mfd plus or minus 10 percent
Load Impedance (L/G)	2000 ohms
Rise and Fall Times	The rise and fall time shall be between 10 and 200 nanoseconds from 10 percent (V2-V1) (See Figure 13) to 3.0 volts after passing through zero volts. The rise and fall times between 10 and 90 percent of the voltage limits shall be between 100 and 1000 nanoseconds. All rise and fall times shall be measured driving 75 ohms plus or minus 10 percent in parallel with 1000 picofarads plus or minus 10%.

3.2.1.4.3.1 Data Output Circuit Characteristics The data output is a differential output voltage. The data output shall be transformer coupled. The output circuit shall be capable of driving no less than 150 feet of cable (see Paragraph 3.2.1.4.2). Skew between signal outputs of the differential driver shall not exceed 30 nanoseconds. The electrical characteristics of the data output signals shall be as follows:

Serial Data Signal Parameter	Characteristics
Positive pulse level (true)	Plus 3 volts to plus 6 volts
Negative pulse level (false)	Minus 3 volts to minus 6 volts
Rise time	60 to 250 nanoseconds
Fall time	60 to 250 nanoseconds
Source Impedance	83 ohms maximum
Load Impedance	75 ohms plus or minus 10 percent
Transmitter voltage baseline recovery	Remain within 75 millivolts of zero volts differential from 5 microseconds after parity until next word sync pattern

Serial Data output voltages shall be peak line to line as measured at the output of the circuit on the signal leads.

Processing of data shall be inhibited following reception of parity bit until the word discrete goes FALSE and then goes TRUE.

NOTE: The rise and fall time shall be measured between 10 and 90 percent of the voltage limits driving a resistive load of 75 ohms plus or minus 10 percent.

3.2.1.4.4 Input Circuit Noise Rejection The data receiver shall detect data and clock signals specified herein that have a signal-to-noise ratio of plus 16.5 dB with a probable bit error of less than one/part in 10^7 prior to the data validation checks. The signal-to-noise ratio shall be determined with 2.0 volt peak, line-to-line signals in message form, as specified herein, and white Gaussian noise distributed over the band of 1000 Hz to 5.0 MHz. The input circuit shall reject all noise at all frequencies up to plus or minus 6 volts peak, line-to-line, below 1000 Hz, and between 5.0 MHz and 30 MHz.

3.2.1.4.5 Input Circuit Common Mode Rejection Signals from dc to 2.0 MHz with amplitudes up to plus or minus 10 volts peak, line to ground applied to both input circuit terminals shall not cause the data receivers to operate.

3.2.1.4.6 Receiver Input Sensitivity The data receiver shall respond with an input signal amplitude from plus or minus 8.0 volts peak line-to-line, down to a threshold level of plus or minus 1.0 volts peak, line to line. The receiver shall not respond to input signals of 0.0 to plus or minus 0.25 volts peak, line to line. The receiver shall operate as specified in Paragraph 3.2.1.4.4 with input signal level of plus or minus 8.0 volts peak, line to line, down to plus or minus 1.5 volts peak plus or minus 10 percent, line to line as measured at the input to the receiver.

3.2.1.4.7 Data and Sync Decoding The receiver shall properly decode data and sync transitions for a combination of received pulse-to-pulse jitter and pulse-width distortion of plus or minus 50 nanoseconds maximum.

3.2.1.4.8 Power Output The transmitter shall be capable of driving the cable specified in Paragraph 3.2.1.4.2 when terminated by 71 ohms ± 10 percent.

3.2.1.4.9 Output Waveform Distortion Any distortion of the waveform of the output circuit, including overshoot and ringing, shall not exceed +250, -150 millivolts peak, line to line.

3.2.1.4.10 Data Transmitter Output Noise When an output channel is selected (channel discretes true), and the FMDM transmitter is not transmitting, the line-to-line noise on all channels shall be less tha 50 millivolts peak-to-peak. When the FMDM is transmitting, the line-to-line noise on unused channels shall be less than plus or minus 300 millivolts peak.

3.2.1.4.11 Transmission Method

3.2.1.4.12 Pulse Code Modulation (PCM) Data and synchronization information shall be transmitted using pulse code modulation (PCM).

3.2.1.4.13 Data Code The data code shall be Manchester II (BiØ-L) as defined in MIL-STD-442. A logic "1" shall be transmitted as a bipolar coded signal (i.e., a positive pulse followed by a negative pulse). (See Figure 14.)

3.2.1.4.14 Data Rate The data bit rate shall be 1-megabit per second, plus or minus 0.1 percent average.

3.2.1.4.15 Clock The clock shall be generated by the transmitting device and used in the fabrication of the Manchester II code format. When receiving data, the FMDM shall derive the clock from the Manchester II code format as received.

3.2.1.4.16 Input/Output Impedance The FMDM shall provide a 71 ohm ± 10 percent input impedance for each serial digital I/O data signal line measured at the FMDM signal interface connections.

3.2.1.4.17 Message Each message shall consist of one or more serial words up to a maximum of 32 words. Each word shall be preceded by a data word sync.

3.2.1.4.18 Data Word Sync The data word sync shall be a nonvalid Manchester code, as shown in Figure 15. The negative and positive going pulses that form a data word sync shall each be 1.5 microseconds, plus or minus 3 percent wide, respectively. A Manchester II/10 code immediately following the data word sync will increase the apparent width of the affected pulse by 0.5 microsecond plus or minus 10 percent.

3.2.1.4.19 Word Size The word size shall be 16 bits, plus 3 bits sync, plus 1 parity bit.

3.2.1.4.20 Word Format The word format (bit definition) shall be as shown below:

3	16	1
Sync	Data	Parity

Serial Channel Word Format

3.2.1.4.21 Serial Channel Operation The serial channel shall be designed for a bidirectional data transfer between the FMDM and subsystem.

3.2.1.4.22 Data Transfer to Subsystem Serial data transmission to subsystems shall be under FMDM control. Operation of data transfer shall be as follows:

- Transmission of data words (16 bits of data plus sync and parity) shall be initiated when the message-out discrete and word discrete are switched to a logic "1" state, and shall be ended when these signals are switched to a logic "0" state.
- The time phasing of the message-out discrete, word discrete, and date word shall be as shown in Figure 12.

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When a multiple-word message is transmitted to a subsystem (32-word maximum), the word discrete shall be toggled between each output word. The message-out discrete shall remain in the logic "1" state during the entire multi-word message. The end of a message shall be indicated by the transition of the message-out discrete from a logic "1" state to a logic "0" state.

3.2.1.4.23 Data Transfer from Subsystem Serial data transmission from subsystems shall be under FMDM control. Operation of data transfer shall be as follows:

- Transmission of data words (16 bits of data plus sync and parity) shall be initiated when the message in discrete and the word discrete are switched to a logic "1" state, and shall be ended when these signals are switched to a logic "0" state.

- The time phasing of the message in discrete, word discrete, and data word shall be as shown in Figure 12.

When a multiple-word message is transmitted from a subsystem (32-word maximum), the word discrete shall be toggled between each input word. The message in discrete shall remain in the logic "1" state during the entire multiple word message. The end of a message shall be indicated by the transition of the message in discrete from a logic "1" state to a logic "0" state. The subsystem will interpret each serial message request as a request to start with the first serial word.

- ~~If~~ the FMDM detects an error on a serial word, the appropriate error bit shall be set as defined in Paragraph 3.2.1.4.24 and the word shall be forwarded to the external device requesting the serial message.

3.2.1.4.24 Data Validation Logic shall be provided in the receiver to recogize the following: (1) improperly coded signals received from the transmitter, (2) data dropouts in the received signals. Each received word shall conform to the following minimum validation criteria:

- The bit orientation in the received waveform reflects a valid Manchester II code (i.e., checks shall be made to determine that only 10 or 01 pattern occurs, and that only the proper number of receiver threshold transitions occur within each bit time). It is intended that this detection of Manchester II waveform anomalies shall provide a high degree of protection against untested message errors due to burst-type noise.

- The word has exactly 16 bits, plus sync, plus parity.
- Parity bit verification

When a word fails to conform to the preceding criteria (i.e., parity, invalid Manchester bit count, no response, or missing words), the word shall be considered invalid. For all cases of error, Bit 26 of the response data word shall be set to a logic "1" state.

3.2.1.5 Interface Protection

3.2.1.5.1 Input Circuitry No signal receiver (analog, discrete, or digital) shall be damaged when any input is shorted to signal, power, or chassis ground, or when its input lines are tied common. No signal receiver (analog, discrete, or digital) shall be damaged when plus or minus 32 volts dc with references to power, chassis or signal ground is applied for an indefinite period of time. During the above conditions all other FMDM I/O signals and FMDM operation characteristics shall not be degraded from the requirements specified herein. A specific exception to this paragraph is called out in Paragraph 3.2.1.4.3.

3.2.1.5.2 Output Circuitry No output circuitry (analog, discrete, or digital) shall be damaged when any output is shorted to signal, power, or chassis ground, or when its output lines are tied common. No signal output circuitry (analog, discrete, or digital) shall be damaged when plus or minus 32 volts dc is applied for an indefinite period to any outputs with reference to power, chassis or signal ground. During the above conditions all other FMDM I/O signals and FMDM operation characteristics shall not be degraded from the requirements specified herein. A specific exception applies to Paragraph 3.2.1.4.1.2.1.3 in that no output protection is required for the application of -32 volts dc or for a short to 28 volts dc power ground. As a design goal, the failure resulting from the shorting to ground or overvoltage application shall be limited to that output, and shall not propagate to other outputs or channels.

No signal output shall provide more than 150 percent of its rated voltage. As a design goal, a fail-safe feature shall be provided for all outputs to fail in a logic "0" output voltage state.

3.2.1.5.3 Input/Output Function Isolation The FMDM shall be designed with an input/output isolation capability so that a failure of one I/O function has no adverse effect on the operation of any other I/O functions.

3.2.1.6 Subsystem I/O Modules I/O modules shall provide the interface between the FMDM and the vehicle subsystems. The modules shall plug into the

FMDM to provide any combination of I/O configurations available from a standard I/O module library. The FMDM shall provide 16 connector slots for these modules that can use all of one type or any combination. Each of the I/O modules shall interface with redundant interface sequence control units. This interface shall be accomplished via dual redundant channels. The FMDM I/O modules shall not contain any mechanically adjustable electrical components. The exchange of one I/O module type for any other I/O module type in any or all of the I/O module locations shall not require changes to or the replacement of any other MDM circuits.

3.2.1.6.1 Addressability The FMDM design shall provide for the addressing of any I/O module or I/O channel at the rate of once per each data bus word time. No restrictions on addressing sequence shall be made.

The address channel (9 bits), as defined by this specification, shall consist of two fields: (a) module address, 4 bit; and (b) module channel address, 5 bits.

3.2.1.6.2 DC Input, Differential or Single-Ended Module The dc input differential module shall receive dc analog signals that have full-scale values of plus zero to plus 5.11 volts or minus 5.12 volts. These inputs shall be from the vehicle subsystems, and shall consist or 32 selectable channels. The module shall provide signal termination, input signal selection, noise suppression or filtering, over-voltage protection, signal isolation, and multiplexing of conditioned signals onto a redundant analog bus for signal transfer to the analog-to-digital module. Electrical characteristic requirements are specified in Paragraph 3.1.2.4.1.1.2.1. The output signals from this module shall be transferred via the PAM line to the A/D module.

3.2.1.6.3 Discrete Input (5-Volt) Module The discrete input (5-volt) module shall receive binary signals. These inputs shall be from the vehicle subsystems, and shall consist of three selectable groups of 16 discretes each. A group of 16 discretes shall be defined as one channel as specified by the five-bit channel address field in the command word (i.e., module n, channel 0, assuming that module n is a discrete input module and channel 0 specified the first 16 discretes of that module). The module shall provide signal termination circuits, signal conditioning, input signal selection, noise suppression or filtering, over-voltage protection, signal isolation, and interfacing circuitry compatible with the sampling of 16-bit data for transfer to the SCU module. Electrical characteristic requirements are described in Paragraph 3.1.2.4.1.1.1.1.1.

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3.2.1.6.4 Discrete Input (28-Volt) Module The discrete input (28-volt) module shall receive discrete binary signals. These inputs shall be from the subsystems, and shall consist of three selectable groups of 16 discretes each. A group of 16 discretes shall be defined as one channel as specified by the five-bit channel address field in the command word (i.e., module n, channel 0, assuming the module n is a discrete input module and channel 0 specified the first 16 discretes of that module). The module shall provide single-ended termination circuits, signal conditioning, input signal selection, noise suppression or filtering, overvoltage protection, signal isolation, and interfacing circuitry compatible with the transfer of 16-bit parallel data from the module for transmission onto the serial data bus. Twenty-eight vdc ground shall be used for the signal return. Electrical characteristic requirements are described in Paragraph 3.1.2.4.1.1.1.2.1.

3.2.1.6.5 Discrete Output (5-Volt) Module The discrete output (5-volt) module shall transmit discrete binary signals. These outputs shall be from the FMDM to the subsystems, and shall consist or three selectable groups of 16 discretes each. A group of 16 discretes shall be defined as one channel as specified by the five-bit channel address field in the command word (i.e., module n, channel 0, assuming that module n is a discrete input module and channel 0 specifies the first 16 discretes of that module). A discrete group binary configuration shall be controlled by the address instruction, and the module shall have set/reset registers for maintaining this configuration until changed by a new command. The set/reset registers shall be such that any or all of the 16 bits of the selected output group (channel) can be changed by the corresponding bit of the command data word. Bits to be changed shall be represented by a logic "1" of the command data word, and shall cause the corresponding bit of the set/reset register to set to logic "1" if a set command is indicated by a logic "1" in bit position 18 of the command word (reference Figure 7). A logic "0" in the bit position 18 of the command word shall represent a reset command, and shall cause the corresponding bit of set/reset register to reset a logic "0"; other bits of the set/reset register shall not be affected. Discrete output drivers shall be single-ended. Electrical characteristics requirements are described in Paragraph 3.1.2.4.1.2.1.1.1.

3.2.1.6.6 Discrete Output (28-Volt) Module The discrete output (28-volt) module shall transmit discrete binary signals. These outputs shall be from the FMDM to the subsystems, and shall consist of three selectable groups of 16 discretes each. A group of 16 discretes shall be defined as one channel as specified by the five-bit channel address field of the command word (i.e., module n, channel 0, assuming that module n is a discrete input module channel and 0 specifies the first 16 discretes of that module). A discrete group

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binary configuration shall be controlled by the address instruction, and the module shall have set/reset registers for maintaining this configuration until changed by a new command. The set/reset registers shall be such that any or all of the 16 bits of the selected output group (channel) can be changed by the corresponding bit of the command word. Bits to be changed shall be represented by a logic "1" of the command word, and shall cause the corresponding bit of the set/reset register to set to logic "1" if a set command is indicated by a logic "1" in bit position 18 of the command word (reference Figure 7). A logic "0" in bit position 18 of the command word shall represent a reset command, and shall cause the corresponding bit of set/reset register to reset to logic "0"; other bits of the set/reset register shall not be affected. Discrete output drivers shall be single-ended. The module shall provide output ground signal, isolation noise suppression, overvoltage limit circuits, and interfacing circuits compatible with transfer of 16-bit parallel data. All signals shall be referenced to a 28-volt power ground. Electrical characteristic requirements are described in Paragraph 3.1.2.4.1.2.1.2.1.

3.2.1.6.7 DC Output Module The DC Output Module shall transmit differential dc analog signals in the range of plus 5.11 volts dc to minus 5.12 volts dc. These outputs shall be from the FMDM to the vehicle subsystems, and shall consist of 16 selectable output channels. The module shall receive a digital data word and shall convert this word to analog dc output in a 10-bit digital-to-analog converter per channel. Each dc output channel shall be provided with a sample-and-hold timing and control circuitry to maintain the dc output accuracy requirements as defined by this document. Design of the module shall be such that no single channel failure shall disable or interfere with any other channel. The module shall provide dc output drivers, noise suppression, overvoltage limiting circuitry, interfacing circuitry, and interfacing circuits compatible with transfer of data from the SCU. Output signals shall be maintained at the selected levels without any requirement for periodic updating from an external device. Electrical characteristic requirements are described in Paragraph 3..2.4.1.2.2.1. Serial delays (from command input to signal changes) within the module shall not exceed 1.0 millisecond.

The FMDM design shall provide for a future requirement of 12-bit DAC.

3.2.1.6.8 Serial Digital I/O Channel Module Each channel shall be a half-duplex channel with electrical characteristics as defined by this specification. The module shall contain four independent serial I/O channels and associated control circuitry. The module shall provide encoding, decoding, temporary data word buffering, parity code checking and generation on all words transferred between serial-digital I/O. The data transfer between FMDM and the

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subsystems shall be on the word-by-word basis, with adequate buffering to match the data transfer on the data bus. The data transfer operation shall be under direct control of the transmitting/receiving FMDM. The module shall provide receiving/driving circuitry, noise suppression, signal coupling, channel protection, and interfacing circuits compatible with transfer of data on the internal data buses.

3.2.1.6.9 Analog-to-Digital Converter The A/D converter module shall digitally encode all analog signals obtained from the nondigital subsystem I/O module. The A/D module shall operate as specified when plugged into either of the two analog-to-digital module locations. It shall be controlled by the SCU for the processing of analog signals. Encoder resolution shall be 10 bits, including sign. Encoder design shall provide for a maximum sampling time of one bit per microsecond.

The module shall provide for transfer of encoded data on the internal data bus.

The sign bit shall be a logic "0" for input signal where the high input is positive with respect to the low or signal return input, and logic "1" if the high input is negative with respect to the low or signal return input. The sign bit shall be placed in Bit 9 of the response data word.

The input signal shall be encoded in binary form and placed in Bits 10 through 18 of the response data word, most-significant bit first.

The A/D shall output a binary 2's complement when the sign bit is logic "1".

The FMDM design shall provide for a future requirement of a 12-bit analog-to-digital module.

3.2.1.6.10 Pulsed Output (28-Volt) Module The pulsed output module shall transmit pulsed discrete signals to the subsystems and shall consist of three selectable groups of 16 outputs each. A group of 16 outputs shall be defined as one channel as specified by the five-bit channel address field of the command word (i.e., module n, channel 0, assuming that module n is a pulsed output module channel 0 specifies the first outputs of that module). The address technique shall be such that any or all of the 16 bits of the selected output group (channel) can be controlled by the command data word. Bits to be pulsed shall be represented by a logic "1" in the command data word, and shall cause the corresponding output bits to be set to the positive pulse level for 20 milliseconds. Bits not represented by a logic "1" shall not be affected. Output drivers shall be single-ended. The module shall provide output ground

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signal, isolation noise suppression, overvoltage limit circuits, and interfacing circuits compatible with transfer of parallel data. All signals shall be referenced to a 28-volt power ground. Electrical characteristic requirements are described in Paragraph 3.1.2.4.1.2.1.3.1.

3.2.1.7 Operating Modes

3.2.1.7.1 Mode Control Upon receipt of the command word, the FMDM shall decode the mode control field (Bits 10 to 13) and execute the following operations: (Refer to Figure 7.)

0001 The FMDM shall read the contents of the EPROM at the address specified by Bits 14 to 22 of the Command Word (CW) and transfer the data to the data bus.

0010 The FMDM shall read out the contents of the EPROM at the address specified by Bits 14 to 22 of the CW, decode the data, and execute the instruction.

0011 SPARE

0100 The FMDM shall execute the BITE 1 test routine (SCU).

0101 The FMDM shall execute the BITE 2 test routine (A/D).

0110 The FMDM shall execute the BITE 3 test routine (Power Supply).

0111 The FMDM shall execute the BITE 4 test routine (IOM).

1000 The FMDM shall prepare to receive the next word/words from the data bus as Command Data Words (CDW). (Refer to Figure 8.)

1001 The FMDM shall be prepared to transfer subsystem received data/internal register data to the data bus as Response Data Word/words (RDW). (Refer to Figure 8.)

1010 The FMDM shall read the contents of the BITE status register and transfer the data to the data bus as a response data word. The BITE status register shall reset itself after each interrogation, or master reset.

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If the first word transmitted following a power transient is BITE status, the "S" indication shall not be given in the SEV field of the response data word. Failures that are still present or reoccur after the BITE registers have been reset shall be indicated again in the BITE status registr.

1011 The FMDM shall set all registers logic "0", all output signals to logic "0", all dc analog outputs to 0-volts, and return to the idle mode.

1100 The FMDM shall return 14 bits of the received CW, starting with Bit 14 and ending with Bit 27. Bits 14 to 27 of the received CW are to be inserted into Bits 9 to 22 of the RDW; Bits 23 and 24 of the RDW shall be loaded with "0"s.

1101 SPARE

1110 The FMDM shall load the BITE status register with the data portion of the next CDW.

1111 SPARE

3.2.1.7.2 Word Sequence Request The FMDM shall have the ability to select up to 512 PROM addresses. Each selected PROM address shall consist of a pre-programmed sequence of input operations for a number of FMDM I/O modules and channel addresses.

The instruction format of each sequence shall conform to the format of the command word (see Figure 7). When an external device requests a specific sequence, the SCU shall execute the requested sequence and then transition to an idle mode.

3.2.1.7.2.1 Sequence Memory The sequence memory shall utilize programmable read-only memory technology. The capacity of the memory shall be 512 words of 16 bits per word. The sequence memory shall be implemented as a separate plug-in module. The memory shall be programmable while mounted within the FMDM. All memory addresses shall be addressable and programmable via an FMDM external connector.

3.2.1.7.2.2 Word Format The word format shall be a direct subset of the command word format. The information fields shall include mode, module address, channel address, and number of words. The word format mode field shall include, as a minimum, the following:

- Prepare FMDM to receive command data
- Prepare FMDM to transmit response data
- Send the BITE status
- Reset the BITE status register
- IOM BITE

3.2.1.8 Response Performance The FMDM shall be capable of transmitting the first response data word on the data bus within 5 to 23 microseconds after receipt of the command word. Subsequent response data words shall be transmitted sequentially, with an interword gap time of 5.5 plus or minus 0.5 microseconds.

3.2.2 Physical Characteristics The FMDM shall have the following physical characteristics.

3.2.2.1 Envelope The envelope of the FMDM shall not exceed the dimensions shown in Figure 2 or Figure 3 as applicable. Connectors shall be on the front panel as indicated by Figure 2 or Figure 3.

3.2.2.2 Weight The weight of the FMDM shall depend upon the FMDM configuration. The FMDM design shall reflect minimal weight. Weights for the configurations specified in Appendix A, TBD.

3.2.2.3 CG and Moments of Inertia The center of gravity (cg) shall be determined in three axes from a defined reference datum. The moments of inertia shall be calculated about the cg for each FMDM configuration. Reference Appendix A.

3.2.2.4 Volume The packaging of the FMDM with all the control elements, modules, radiator, optional cold plate surface and power supplies shall reflect the envelope constraints of Figures 2 or 3.

3.2.2.5 Surface Wear Interacting surfaces in the FMDM shall be sufficiently smooth and wear resistant so that particle generation will not preclude the normal functioning of the item as specified herein.

3.2.2.6 Power Supply Packaging The power supply shall be divided into sections, with only the heavier core supply section secured to the rear panel.

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3.2.3 Reliability

3.2.3.1 Failure Deterrent and Detection The design shall incorporate the following:

- Alternate or redundant means of performing a critical function shall be physically separated by the maximum practical distance, or otherwise protected so that all functional paths will not be lost due to a single event.
- The FMDM shall be designed so that transient out-of-tolerance conditions or component failures will not cause other component/subsystem failures.
- Redundant components susceptible to similar environmental failure cases (such as shock, vibration, acceleration, or heat loads) shall be physically oriented or separated to reduce the chance of multiple failure from the same cause(s).
- Design shall provide for isolation of anomalies of identified critical functions so that a faulty subsystem or Line Replacement Unit (LRU) can be deactivated either automtically or by manual selection without disrupting its own or other subsystems.
- Where similar connections are in close physical proximity, the design shall preclude the capability of cross-connection.
- Solid state switches and amplifiers shall be given preference over electro-mechanical relays and other vibration-sensitive electrical/electronic parts. Scaled-type terminal blocks shall not be used.
- When there is an indication that an event necessary to continuation has failed to occur, the capability to determine status of sub-events shall be provided.
- Threaded parts and fasteners shall be positively locked to prevent loosening during service.
- Unidirectional components or piece parts shall be designed to preclude backward installation by using non-symmetry of configuration, different connecting sizes, or comparable means.

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- Bypass circuits used in checkout or calibration procedures shall not override electrical system protective devices.

- Redundancy shall be designed in accordance with MF0004-002 so that the redundant paths may be verified externally to the component closure.

3.2.4 Maintainability

3.2.4.1 Design Allocations The design shall satisfy the following maintainability allocations:

a. The FMDM shall have the ability, in conjunction with Ground Support Equipment (GSE) if applicable, to isolate any discrepancy to the malfunctioning LRU or onboard verification of LRU functional performance after installation within 20 minutes.

b. Scheduled maintenance required for equipment shall be limited to replacement of time/cycle sensitive equipment.

c. The FMDM shall be designed to allow failed subassemblies to be replaced in 0.5 hours or less after failure identification.

d. The FMDM shall be designed to allow bench verification of the electrical interfaces and module functions within 3.0 hours, using suitable support equipment in the maintenance area.

e. The FMDM acceptance test equipment shall have the ability to perform functional acceptance and/or fault isolation testing on FMDMs having any and all possible I/O module configurations with a common test adapter and software package.

3.2.4.2 Design Features The design shall incorporate the following maintainability features.

3.2.4.2.1 Maintenance

a. The FMDM shall not require scheduled maintenance except as noted in 3.2.4.1(b).

b. The FMDM shall be designed to preclude the use of special tools and equipment for site maintenance and repairs. Special tools, if required and approved by the buyer, shall be designed to withstand the intended use throughout the life of the equipment.

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c. FMDM shall be designed so that routine corrective maintenance can be accomplished by the replacement of Shop Replaceable Units (SRUs). The FMDM design shall be such that isolation to a single malfunctioning SRU can be accomplished during bench maintenance. The addition of test points to the system interface connectors or the addition of a system GSE test connector is permissible, with buyer's approval, to provide this capability.

d. SRUs shall be designed so that maintenance actions not requiring extensive refabrication, refurbishment, or overhaul can be accomplished at the shop level of maintenance. Corrective maintenance of SRUs shall be accomplished by the replacement of minor subassemblies or piece parts. SRUs shall be designed to preclude the loss or dropping of hardware which could cause internal damage or affect the FMDM's serviceability or increase maintenance time.

e. Scheduled maintenance of the FMDM when in its installed configuration shall be limited to the maintenance and repair areas.

f. On-line testing (BITE) shall be the only test capability to be accomplished during flight.

g. No on-vehicle adjustments or calibration shall be required.

h. Suitable warnings shall be provided on instruction plates or service placards if hazardous conditions exist when maintenance is performed.

i. The FMDM design shall not require pre-installation acceptance checkout prior to use.

j. The FMDM shall be designed so as to preclude the need for on-line support equipment.

3.2.4.2.2 Installation

a. The equipment design shall physically prevent the incorrect installation of modules and sub-modules.

b. Components shall be mounted in a manner to avoid blind matings.

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c. Mechanical retention devices for equipment/components shall not require safety wiring.

d. If an FMDM is mounted and secured by bolts where the component must be held in place until the bolts are engaged, pilot keyhole mounting or similar installation aid shall be provided.

e. Where practical, threaded fasteners used for securing a single component shall be the same type, size, and tensile strength.

f. Assembly/subassembly installation shall be designed so that accessibility to threaded fasteners may be accomplished without the use of universal joints, angular extensions, handle extensions, or combinations thereof, in conjunction with torque tools.

3.2.4.2.3 Accessibility

a. Electrical connectors shall be accessible without disassembly or removal of functional equipment or components.

b. Servicing and test points shall be clearly marked, and shall be accessible without requiring removal of access plates or covers except service caps.

c. All fasteners on a single access cover shall be of the same length, diameter, and type.

3.2.4.2.4 Replacement Mounting provisions shall permit SRU removal and replacement without disconnecting any equivalent level SRU in the FMDM. If removal of an FMDM structural element is required for access, such removal shall not affect electrical or mechanical alignment, nor shall the mechanical strength of the unit be impaired to the point that bending of the unit, its assemblies, electrical harnesses, or plumbing attachments will occur during normal bench handling of the unit.

3.2.4.2.5 Handling

a. Handling provisions shall be provided on FMDMs in accordance with MIL-STD-1472.

b. All wiring harnesses shall be protected from handling damage. The protective considerations shall not inhibit repair or replacement of the wire harness.

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3.2.4.3 Self-Test Provisions

3.2.4.3.1 General Requirements The FMDM shall contain the necessary built-in-test capability to detect and report failures which affect operation. This built-in-test ability (in conjunction with the integrated avionics) shall provide the means for accomplishing functional path failure detection during flight along with the necessary FMDM fault isolation to support ground turnaround requirements. The built-in-test ability, when augmented by integrated avionics, shall provide a 0.96 probability of failure detection at the LRU level, and shall not require demating of connectors or connecting of carry-on GSE.

3.2.4.3.2 Self-Test Capability

3.2.4.3.2.1 Built-In-Test Equipment (BITE) The BITE shall be implemented to achieve a probability of 0.96 (excluding the MIA), or better, for detecting failures or out-of-tolerance conditions of the FMDM modules, as defined in Paragraph 3.2.1.6. BITE functions consist of (but are not limited to) the following:

a. On-line monitoring

b. BITE tests

Results of a. and b. are stored in the BITE status register.

3.2.4.3.3 On-Line Monitoring Candidates for on-line monitoring consist of, but are not limited to:

- Parity and cyclic code checking on microprograms/control stores
- Parity checking on PROM operations; internal data transfers
- Input/output module control functions
- Monitoring of MIA validity and fault lines and FMDM/MIA power supplies

FMDM monitor functions require no initiation (i.e., no instructions).

3.2.4.3.4 Bite Tests Implementation BITE tests shall be initiated under control of GPC/PCM commands.

Test routines may be stored in FMDM PROMs or in GPC/PCM main stores. Test routines for FMDM timing, input tests, serial input/output wraparound may be under control of PROM stored instructions. BITE test instructions are not to cause any FMDM subsystem output signal to change state except for the serial input/output lines during BITE test.

DC analog outputs and discrete outputs shall be tested under GPC/PCM control. The FMDM shall provide for sampling these outputs without interfering with their programmed output state. The sampled data shall be forwarded to the GPC/PCM for comparison with the programmed output.

3.2.4.3.5 BITE Status Register The BITE status register shall be used to report FMDM monitored conditions and BITE results to the GPC. All monitored fault conditions, except for power applied/interrupt, set the validity bit to a pre-determined state in a response word (Bit 27), indicating to the GPC/IOP that the BITE status register should be interrogated. Power applied/interrupt corresponds to Bit 25 of a response data word. The BITE status register is reset after GPC/IOP interrogation or by a commanded FMDM master reset. When the FMDM receives a request for BITE status, the response data word Bit 25 shall be set to "1", Bit 26 shall be set to "0", and Bit 27 shall be set to "1."

The BITE status register bit assignment shall be as shown in Figure 16.

3.2.4.3.6 Test Circuitry Failure The test circuitry shall be fail-safe, and shall not induce failures in other portions of the LRU or in another LRU.

3.2.5 Environments

3.2.5.1 Operational The FMDM shall be capable of meeting the operating performance requirements specified herein during and after exposure to any feasible combination of the following conditions:

a. Temperature (cold plate cooling)	Minimum:	Minus 65°F (Minus 54°C)
	Maximum:	Plus 160°F (Plus 71°C)
Temperature (radiation cooling)	Minimum:	Minus 207°F (Minus 133°C)
	Maximum:	Plus 159°F (Plus 70.5°C)

As a design objective, the FMDM will operate as specified herein (in the radiation cooling mode) when mounted to surfaces which have temperatures ranging from +120°C to -155°C.

Note: Worst-case low temperature ambient is defined by the average tail-to-sun condition of Figure 4.6, Page 4-16D of the Change 20, Volume XIV, Space Shuttle System Payload Accommodations, JSC 07700. Worst-case high temperature ambient is defined by the average top-to-sun conditions of the same reference document. Temperature extremes specified for a radiation cooled case above are for empty payload bay sidewall surfaces.

b. Pressure — Minimum: 10^{-11} Torr (1.33×10^{-9} N/m^2)
Maximum: 18.0 psia (1.241×10^5 N/m^2)

c. Humidity — Minimum: 0 percent, relative
Maximum: 100 percent, relative

d. Salt Fog — Exposure to one percent salt solution by weight.

e. Lightning — In accordance with MF0004-002 for indirect effects

f. Random Vibration

(1) Qualification - Acceptance Vibration

20 - 80 Hz plus 3 dB/octave to 0.067 G^2/Hz at 80 Hz
80 - 350 Hz at 0.067 g^2/Hz
350 - 2000 Hz minus 3 dB/octave from 0.067 g^2/Hz at 350 Hz

Duration: 5 times the duration of AVT (See 4.2.4.1.6.1)

(2) Flight

10 - 40 Hz	Constant at 0.04 g^2/Hz to 40 Hz
40 - 75 Hz	Increasing at 6 dB/octave to 75 Hz
75 - 200 Hz	Constant at 0.15 g^2/Hz to 200 Hz
200 - 270 Hz	Decreasing at 6 dB/octave from 0.15 g^2/Hz at 200 Hz
270 - 900 Hz	Constant at 0.09 g^2/Hz to 900 Hz
900 - 2000 Hz	Decreasing at 9 dB/octave from 0.09 g^2/Hz at 900 Hz

Duration: 48 minutes per axis

g. Acceleration

Plus and minus 5 g's in all major axes

h. Deleted

i. Explosive Atmosphere. Explosion-proof design shall comply with the requirements of MIL-STD-810, Method 511, Procedure I, with butane used for fuel.

j. Solar Radiation (Thermal) Temperature extremes for items exposed to space environments cannot be categorically defined. When determining these extremes analytically, use the data below:

Environmental Parameter	Design Value
Solar Radiation	443.7 Btu/Ft^2/hr
Earth Albedo	30 percent
Earth Radiation	77 Btu/Ft^2/hr
Space Sink Temperature	0° Rankine

3.2.5.2 Non-Operational The FMDM shall be capable of meeting the operating performance requirements specified herein after exposure to the following conditions:

a. Temperatures — Minimum: Minus 65°F (Minus 54°C); Maximum: Plus 250°F (Plus 121°C)

b. Pressure — Minimum: 1 x 10^{-11} torr (1.33 x 10^{-9} N/m^2); Maximum: 30.0 psia (2.068 x 10^5 N/M^2)

c. Sand and Dust

(1) As encountered in desert and ocean beach areas, equivalent to 140-mesh silica flour with particle velocity up to 500 feet per minute and a particle density of 0.25 grams per cubic foot.

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d. Shock

(1) Bench Handling — As specified in MIL-STD-810, Method 516.1, Procedure V.

(2) Basic Design — 20 g terminal sawtooth shock pulse of 11 ms duration in each of three orthogonal axes (both directions).

(3) Crash Safety — 40 g terminal sawtooth shock pulse of 11 ms duration in each of three orthogonal axes (both directions). Equipment and its mounting attachments shall not break loose, create a hazard to personnel, or prevent egress from a crashed vehicle. Operating performance is not required after this test.

e. Ozone — 3 to 6 parts per hundred million (phm). Total oxidant concentrations may reach 60 phm for 1 to 3 hours in any 24 hour period.

f. Fungus — As specified in MC999-0096.

3.2.5.3 Transportation and Storage. The FMDM shall be protected from the environments specified in Paragraph 5.2.3 by adequate packaging or protective processes unless vehicle flight requirements precludes the need.

3.2.6 Transportability. The FMDM shall be designed to be capable of being handled and transported to using facilities without damage or degradation, using available methods of transport, with the item prepared for shipment in accordance with Section 5 requirements. The equipment design shall be compatible with the planned packaging and transportation system to the extent that loads induced in the equipment during transportation will not produce stresses, internal loads or deflections that could result in damage to the equipment.

3.2.6.1 Tiedown Capability. The equipment design shall incorporate structural provisions adequate to permit the hardware to be secured to the transport vehicle, device or container by bolting, blocking, strapping, or other feasible means.

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3.2.6.2 Integral Protective Capability The equipment design shall incorporate one or more of the following provisions for protection of components that are highly vulnerable to damage during transport and associated handling:

- Provide attach points for installation of temporary protective device (covers, reinforcing structure, desicant cartridge, air breather/filter heater, etc).
- Make provisions for removal of sensitive components(s) for separate shipment.
- Provide "built-in" protective device (e.g., cover, caging of free-moving components, desicant chamber, heater, etc).

3.3 Design and Construction

3.3.1 Materials, Processes, and Parts

3.3.1.1 Materials and Processes Materials and processes for the FMDM shall be in accordance with MC999-0096 to the extent specified in the requirements table of the purchase order.

3.3.1.2 Parts Standardization Parts utilization shall be based upon:

- Selection of qualified parts
- Proper derating and application
- Minimizing the number of part types

Parts used in design and fabrication shall be selected from MF0004-100 and MF0004-400.

3.3.1.3 Threads and Fasteners Shall be in accordance with MF0004-100 and MF0004-002.

3.3.1.4 Material Compatibility Materials and processes used in fabrication of the FMDM shall be compatible with the environmental conditions specified herein. The FMDM shall be capable of operation without causing ignition of that atmosphere. The FMDM shall be explosive-proof, and the surface temperature of internal components and the surface temperature of the case shall not exceed 352°F.

3.3.2 Selection of Specifications and Standards Specifications and standards for use in the design and construction of the FMDM, other than those specified herein, shall be selected in the order of precedence in accordance with MIL-STD-143, except that the NASA documents, when suitable for the purpose, shall take precedence.

3.3.3 Electromagnetic Compatibility and Electrical Design

3.3.3.1 Electromagnetic Compatibility (EMC) The generation of electromagnetic interference by the FMDM and the susceptibility of the FMDM to such interference shall meet the requirements of MF0004-002 for Class ID equipment. In addition, the FMDM shall be designed to meet specification requirements when exposed to the Orbiter transmitter frequencies listed below:

Frequency	Exposure Level Volts/Meter
250-300 MHz	4
2200-2300 MHz	8
13-15 GHz	45

3.3.3.2 Electrical Equipment Design The FMDMs shall comply with the general electrical design, development, and test requirements applicable to the Orbiter subsystems, equipment, and components in accordance with specification MF0004-002, to the extent specified in the procurement package.

3.3.3.2.1 Power Consumption Power dissipated by the FMDM with 28 vdc supplied shall be as defined below.

1. Maximum power shall be established under the following operational criteria.

   a. 50 percent of input/output transfers are controlled by sequence control memory and 50 percent are controlled by the SCU.

   b. 40-millisecond iteration time.

   c. 33.5-microsecond word time.

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d. 24 data bus words per iteration.

e. The number of words transferred by IOM per iteration are:

DCIN 13
DI5 3
DO5 3 (average load current = 5mA)
DI28 3
DO28 3 (average load current = 7mA)
DCO 13 (average load current = 4mA)
SD 80 (10 words per channel, in and out)
PO28 3 (average load current = 35 mA)

f. Output IOMs at 35 percent high state.

2. Minimum power shall be with FMDM at idle and all input and output states low.

3. Power dissipation in watts for the OFT Flight FMDM units.

a. Idle (all input and output states low) - TBD watts

b. Maximum (as per Item 1, above) - TBD watts

3.3.3.2.2 Metals and Metal Couples, Restriction on Use Metal joints that require electrical bonding shall be precise, dry, and conducting. Nonconducting corrosion inhibitors may be added after joint assembly. Conducting metal joints shall be required for electrical circuit fault-current return, electrostatic corona prevention, and structural shielding from lightning-strike induction and avionic interference.

3.3.3.2.3 Electrical and Electronic Piece-Parts, Closure Construction Electrical and electronic piece parts with all-welded closure construction shall be used in preference to piece parts with other types of closure construction. Other types of construction may be used if adequate program controls are imposed to assure that internal contamination cannot cause part degradation and failure under a zero-gravity environment.

3.3.4 Identification and Marking

3.3.4.1 Identification of Parts Each fabricated part shall be identified with a part number. The same specification or part number shall be used to identify all like materials, processes, and parts. Seller shall assign a new

part number to the part when authorized changes make the superseded part not interchangeable with respect to interface, reliability, safety, logistics, traceability or performance. For traceable items, the part identification shall additionally include the manufacturer's identification code in accordance with DoD Handbook H 4-1, and be lot/numbered or serial numbered when required.

3.3.4.2 Identification of All Development/Qualification Test Specimens Test specimens shall be permanently and obviously identified prior to testing with the words ENG. TEST ONLY in addition to the identification required by the drawing/specification to preclude their use on production items. The letters shall be indelible, and provide a distinctive and vivid contrast to the color of the specimen. The lettering size and identification location shall be clearly visible to casual observation. Materials used for the identification shall be compatible with the test specimen and its operating environment. When the size or configuration of the test specimen is such that the identification cannot appear on the specimen, other suitable means, such as attached metal tags, shall be used.

3.3.4.3 Nameplates Nameplates shall be marked in accordance with MIL-STD-130, and shall include (as applicable) item name; Federal North Atlantic Treaty Organization Stock Number (FSN/NATO); manufacturer; date of manufacture; and manufacturer's serial number, part number, lot number, and code identification number. Abbreviations, in accordance with MIL-STD-12, may be used.

3.3.5 Interchangeability The FMDM and the items identified in 3.1.3 shall be interchangeable in accordance with the definition of MIL-STD-280. Interchangeability shall be a design feature for all removable items/subassemblies/parts designated as LRUs or SRUs. When removable items/subassemblies contain controls, wiring, etc, interchangeability shall be provided at the attachments of these items to their next assembly and for structural attachments of the assembly.

3.3.5.1 Design Tolerances Provisions shall be made for design tolerances so that items having the dimensions and characteristics permitted by the item specification or drawing are interchangeable without selection or departure from the specified equipment performance.

3.3.5.2 Use of Standard Parts When standard parts (refer to 3.3.1.2) are not available, and permission is granted for use of a non-standard part due to unavailability of the standard part, the equipment shall be designed so that

the non-standard part can be replaced by the standard part. Appropriate space, mounting holes, and other necessary provisions shall be provided for this purpose.

3.3.6 Safety The design and operation of the FMDM shall comply with the following safety requirements:

a. Transient effects to the FMDM cannot introduce erroneous signals that are hazardous during critical operations.

b. The FMDM shall not generate electrical current or radio frequency transients that could cause failure or malfunction of other equipment unless the FMDM is properly shielded.

c. The physical form or shape, as designed and built, shall minimize sharp surfaces or protrusions which present a hazard to operations personnel or to their personal clothing or equipment. When such features are required for mission accomplishment, then suitable guards shall be provided for ground or flight-handling operations.

3.3.7 Human Performance/Engineering The design shall consider the abilities and limitations of the human operator wherever a man-machine interface exits, including torques, forces, and other functional design characteristics of controls, displays, and work stations. The principal design guide for the man-machine interface shall be MIL-STD-1472. Handling provisions shall be in accordance with 3.2.4.2.5.

4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

4.1.1 General Verification Guidelines and Criteria The seller shall use the following general requirements in developing a verification program.

a. Each performance and design requirements specified in Sections 3 and 5 of this specification shall be verified by test, assessment, or analysis in support of certification of the design for operational use.

b. Verification of maintainability, accessibility, and ease of operation shall be demonstrated.

c. Early subsystem integration with the software shall be a key test-program goal.

d. As a general guideline, off-limit testing will not be conducted. However, off-limit testing will be considered:

- When design margins are relatively small with respect to off-nominal abort conditions.
- When uncertainty exists in the definition of the design criteria.
- When single-point failure modes exist.

Testing of this nature must have prior approval of the buyer, and must have considered preservation of at least one specimen of certification hardware for later testing.

e. Acceptance test procedures, equipment, and test levels shall be verified during development testing.

f. Certification shall be structured to verify the full range of the design requirements under specified environments.

g. Wherever practical and technically sound, accelerated life-test techniques shall be used.

h. Testing shall be conducted at the most cost-effective level of assembly.

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i. All qualification test specimens shall be processed through specified acceptance testing prior to qualification test.

j. Where redundancy in design exists, each redundancy shall be verified through normal output sources designed for that purpose.

k. When similar parameters have been verified during Orbiter MDM or SRB MDM programs, the parameter may be verified for this item by similarity that is supported by analysis.

4.1.2 Test Conditions

4.1.2.1 Standard Test Conditions Environmental standard test conditions for tests required by this specification shall be an atmospheric pressure of 28.5 plus 2 or minus 4.5 inches of mercury (Hg), a temperature of 73 plus or minus 18F and a relative humidity of 50 plus or minus 30 percent.

4.1.2.1.1 Coldplate or Forced Air Cooled Equipment When operation of the unit under test is required during environmental exposure, coolant in accordance with specification requirements shall be supplied. During tests in which the ambient temperature is other than standard room ambient, the coolant temperature shall be at design extremes and "in phase" with the test chamber temperature. If the use of coolant will have no effect upon test results for a particular environment, the requirement to use cooling shall be at the discretion of the seller.

4.1.2.1.2 Coldplate Temperatures The average coldplate surface temperature range for coldplate-cooled equipment shall be as follows, unless otherwise specified herein:

Normal Test Range	Acceptance Thermal Test	Qualification Thermal Test
Plus 55 F to plus 80 F	Plus 35 F plus ΔQ to plus 120 F plus ΔQ	Plus 35 F plus ΔQ to plus 120 F plus ΔQ

The average coldplate surface is defined as the surface area enclosed by the perimeter of the test article that interfaces with the coldplate.

ΔQ is the thermal rise resulting from the heat dissipation of the test article, and is determined as:

$$\Delta Q = 5 \text{ F } X(\text{average equipment heat dissipation}) \quad \frac{\text{Watts}}{\text{Sq. In.}}$$

4.1.2.2 Test Tolerances Test tolerances shall be used as specified in MIL-STD-810, or FED-STD-101 as applicable, except as follows:

4.1.2.2.1 Random Vibration Test tolerances and procedures shall be in accordance with SP-T-0023.

Analog Vibration Spectral Density Analysis Criteria Analysis sample time (T) shall equal or exceed 50/BW where BW is the effective bandwidth of the filter used. For swept-filter analysis, analyzer filter scan rate (SR) shall (1) not exceed BW/T (Hz/second) when averaging is obtained using linear integration with an integration time of T, or (2) be BW/4 RC when averaging is obtained by smoothing with an equivalent resistance capacitance (RC) low-pass filter that uses a time constant $RC \geq T/2$.

4.1.2.2.2 Shock (acceleration vs time)	Peak amplitude:	Plus or minus 10 percent
	Pulse duration:	Plus or minus 10 percent
4.1.2.2.3 Acceleration	Specified acceleration:	Plus 10 percent Minus 0 percent
4.1.2.2.4 Exposure Time	Duration specified for vibration or acceleration environments:	Plus 10 percent, minus 0 percent.

4.1.2.2.5 Measuring Instrumentation Allowable error shall not exceed one-tenth of the tolerance specified for the parameter to be measured.

4.1.3 Test Responsibility and Location The seller shall be responsible for implementing the quality assurance requirements specified herein. Except as otherwise noted, the seller may use his own facilities or any commercial laboratory acceptable to the buyer.

4.2 Quality Conformance The following sections define the tests, analyses, simulations, and assessments necessary to verify that the requirements of Sections 3 and 5 of this specification are met.

4.2.1 Development The seller shall perform development encompassing engineering evaluation of hardware, software, manufacturing processes, and techniques for the purpose of acquiring engineering data; identifying sensitive parameters; evaluating the development configuration; providing the necessary

confidence that the hardware will meet the specification requirements; plus assure that the manufacturing process will produce an acceptable product. Development objectives shall encompass the following as a minimum:

a. Design and performance capability, including redundancy.

b. The ability to meet specified requirements with adequate design margin.

c. Integration of each component and subsystem with other components subsystems, facilities, support equipment, etc.

d. Establishment of process, procedures, equipment, and test levels for manufacturing acceptance testing, maintenance, checkout, and operational phases of the program.

e. Identification of significant failure mode and effects.

f. Determination of the effect of various combinations of tolerance and drift of design parameters.

g. Determination of the effect of combinations and sequences of environments and varying stress levels.

h. Identification of safety hazards, parameters, requirements, and procedures.

i. Where similar activities were performed for Orbiter or SRB MDM, such activities need not be repeated for this item.

4.2.1.1 Operating Limits on Temperature-Controlled Equipment For flight equipment whose operating temperature is normally controlled by heating or cooling equipment, and whose temperature is monitored in flight, the test program and appropriate analyses shall define:

a. The maximum and minimum temperatures expected in normal operations.

b. The maximum and minimum temperature at which equipment may be expected to fail to function until temperature is restored to normal range.

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4.2.2 Acceptance Acceptance tests and inspection shall be performed on all FMDMs to be employed in test programs and on all FMDMs delivered to the buyer. The seller shall perform any other test deemed necessary, subject to approval by the buyer. The final tests and inspections shall be performed in a manner and under conditions which simulate end use to the highest degree practicable without damage to the units. The degree, duration, and number of tests shall be sufficient to verify the acceptability of the device for the intended use. Prior to delivery, and as a condition of acceptance, the seller shall conduct the inspection and tests shown in Table I on each FMDM.

TABLE I

ACCEPTANCE REQUIREMENTS

Inspection and Test	Paragraphs Listed in Recommended Sequence
Examination of Product	4.2.2.1
Insulation Resistance Test	4.2.2.6
Dielectric Strength Test	4.2.2.7
Acceptance Vibration Test	4.2.2.3
Acceptance Thermal Test	4.2.2.4
Performance	4.2.2.2
Power Variation Test	4.2.2.8

NOTE: Functional/continuity tests of 4.2.2.2 shall be conducted on each equipment before, during, and after the acceptance vibration tets and acceptance thermal test. When complete functional verification with environments cannot be accomplished during the acceptance test because of limited test time, the most critical functions shall be tested and all other functional circuits monitored.

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4.2.2.1 Examination of Product Each FMDM shall be carefully examined to determine conformance to the requirements of this specification. Particular attention shall be given to weight, workmanship, finish, dimensions, construction, cleanliness, identification, marking, traceability level, and that certified materials and process have been used.

4.2.2.2 Functional and Performance Test Functional and performance tests shall be conducted on all deliverable equipment to establish compliance with the requirements of Section 3. Tolerance bands or pass-fail performance criteria, based on performance design requirements, shall be established for each parameter.

4.2.2.2.1 LRU Equipment Tests Each FMDM submitted for acceptance shall be subjected to individual tests. These tests shall be adequate to determine compliance with the performance requirments specified herein.

4.2.2.2.2 SRU Equipment Tests All SRUs, whether delivered as a module or as component parts, shall be reqired to pass comprehensive acceptance tests in accordance with the acceptance test specification prior to delivery, or, if applicable, assembled as a part of the equipment.

4.2.2.2.3 Testing Below SRU Level Subassemblies, components, piece parts, and other items below the SRU level that are deliverable items shall be required to pass the seller's production tests normally required for such items. Such testing shall ensure form fit and function interchangeability with like items assembled into the equipment.

4.2.2.3 Acceptance Vibration Test The FMDM shall be subjected to random vibration on each of three orthogonal axes in accordance with the spectral density envelope specified below. The vibration duration shall be adequate to perform selected functional performance tests, but shall not be less than 30 seconds or greater than 5 minutes per axis. Should retests be required in any axis, the total accumulative vibration test time shall not exceed the qualified time for AVT in that axis (reference 4.2.4.1.6.1) without prior buyer approval. Tolerances, procedures, and test criteria for vibration shall be in accordance with SP-T-0023.

Acceleration Spectral Density	
20 to 80 Hz	Increasing, at plus 3 dB/octave, to 0.04 g^2/Hz at 80 Hz
80 to 350 Hz	Constant at 0.04 g^2/Hz
350 to 2000 Hz	Decreasing, at minus 3 dB/octave, from 0.04 g^2/Hz at 350 Hz

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4.2.2.4 Acceptance Thermal Test (ATT) The FMDM shall be thermal cycled from 70 F, to plus 145 F to minus 45 F, to plus 145 F, and to 70 F with continuity monitored throughout. The rate of change shall not exceed 240 F per hour, nor be less than 60 F per hour. Dwell at each limit temperature shall be a minimum of the time required to stabilize the device temperature plus the time required to conduct the performance tests; however, the time shall not be less than 1 hour. The performance test at each high-temperature extreme shall include operation at the maximum heat dissipating mode in accordance with 3.3.3.2.1 for a duration consistent with the design capability and sufficient to obtain test data. During the low-temperature extremes, the performance test shall include operation at a minimum power consumption for a duration sufficient to verify acceptable performance. The tolerances and criteria of SP-T-0023 shall apply. Coldplate temperatures shall be in accordance with Paragraph 4.1.2.1.2.

4.2.2.5 Insulation Resistance Test Insulation resistance test shall be in accordance with MF0004-002.

4.2.2.6 Dielectric Strength Dielectric strength test shall be in accordance with MF0004-002 with the exception that the test shall be conducted at 500 volts.

4.2.2.7 Power Variation and Usage Tests Tests shall be conducted to determine if the equipment performs satisfactorily under power input conditions specified in 3.1.2.1.

4.2.3 Assessment Verification by assessment methods shall be used to verify design features. These methods employ the orderly review and evaluation of design documentation or visual inspection techniques (e.g., mock-up forms, fit checks, maintainability access, tolerances, safety wiring and placards).

4.2.3.1 Maintainability Compliance with the maintainability requirements of 3.2.4 which cannot be verified by analysis shall be verified by assessment of engineering data.

4.2.3.2 Materials and Processes Conformance of the FMDM with materials and processes in accordance with 3.3.1.1 which cannot be verified by test or analysis shall be verified by assessment of design drawings and process specifications.

4.2.2.3 Parts Standardization Conformance of the FMDM with standard parts in accordance with 3.3.1.2 shall be verified by assessment of design drawings.

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4.2.3.4 Selection of Specification and Standards Verification that selection of specifications and standards are in accordance with 3.3.2 shall be verified by assessment of design drawings and specifications.

4.2.3.5 Electrical Design Requirements Verification that the FMDM conforms to the electrical design requirements of 3.3.3.2 which cannot be verified by analysis or test shall be verified by assessment of design drawings.

4.2.3.6 Interchangeability Verification that the FMDM design conforms to the interchangeability requirements of 3.3.6 shall be verified by assessment of design documentation.

4.2.3.7 Design Tolerances Verification that the FMDM conforms to the design tolerances required in 3.3.6.1 shall be verified by assessment of the design documentation.

4.2.3.8 Use of Standard Items Verification that standard items will be used in the FMDM when available in accordance with 3.3.6.2 shall be verified by assessment of design drawings.

4.3.3.9 Human Performance/Human Engineering Verification that the FMDM conforms to the human performance/human engineering requirements of 3.3.7 shall be verified by assessment of the design drawings.

4.2.3.10 Reliability Verification of the applicable reliability failure deterrent and detection requirements of 3.2.3.1 which cannot be verified by test or analysis shall be verified by assessment.

4.2.4 Certification The seller shall certify the requirements of Sections 3 and 5 by the methods specified below.

4.2.4.1 Qualification Tests Qualification testing performed to satisfy the requirements specified in the performance and design verification matrix (Table III) shall be in conformance with the requirements of this paragraph. Qualification test specimens shall be subjected to the tests specified in Table II in the sequence shown. Where the specified environment for this item is equal or less severe than that required for the Orbiter or SRB MDM and design differences do not exist; this item shall be qualified by similarity.

TABLE II

REQUIRED TESTS

Test	Paragraph
Acceptance Test (ref)	4.4.2
Power Test	4.2.4.1.10
EMC	4.2.4.1.12
Salt Fog	4.2.4.1.4
Humidity	4.2.4.1.3
Thermal Cycle	4.2.4.1.14
Vibration	4.2.4.1.6
Acceleration	4.2.4.1.7
Thermal Vacuum	4.2.4.1.13
Life	4.2.4.1.14
Explosive/Corrosive Atmosphere	4.2.4.1.9
Lightning	4.2.4.1.11
Shock	4.2.4.1.8

4.2.4.1.1 Test Hardware Qualification test hardware shall be of the same configuration as flight hardware.

4.2.4.1.2 Performance Requirements The EMDM shall be subjected to complete performance tests before and after each environment test, and to selected functional and performance tests during each environmental exposure. Where complete performance verification cannot be accomplished during the environmental exposure because of limited test time, the most critical functions shall have priority. Tolerance bands or pass-fail performance criteria, based on performance design requirements, shall be established for each parameter. Parameter shifts during or after each environment shall not exceed the absolute value of the allowable difference between the acceptance

and qualification test limits for each parameter. Susceptibility of the FMDM to the Orbiter transmitter frequencies specified in Paragraph 3.3.3.1 shall be by test.

4.2.4.1.3 Humidity Test The FMDM shall be subjected to a humidity test in accordance with MIL-STD-810, Method 507, Procedure IV, except performance tests shall be conducted during the second and fourth cycles.

4.2.4.1.4 Salt Fog The FMDM shall be subjected to a salt-fog test in accordance with MIL-STD-810, Method 509, Procedure I.

4.2.4.1.5 Random Vibration

4.2.4.1.5.1 Qualification-Acceptance Vibration Test (Q-AVT) The FMDM shall be subjected to the random vibration specified in 3.2.5.1f(1) for the duration specified, in each of three orthogonal axes. Vibration tolerances, criteria, and test procedures shall be in accordance with SP-T-0023. Performance verification tests shall be identical to those conducted during AVT (reference 4.2.2.3).

4.2.4.1.5.2 Flight Vibration The FMDM shall be subjected to the random vibration specified in 3.2.5.1f(2), for the duration specified, in each of three orthogonal axes. Vibration tolerances, criteria, and test procedures shall be in accordance with SP-T-0023. Performance tests shall be in accordance with 4.2.4.1.2.

4.2.4.1.6 Acceleration The FMDM shall be subjected to the acceleration specified in 3.2.5.1g for a minimum of 5 minutes in each direction along each of the three orthogonal axes. If any axis(es) is (are) considered significant, with respect to acceleration effects, it (they) shall be considered when establishing the orthogonal axis system.

4.2.4.1.7 Shock

a. Bench Handling The FMDM shall be subjected to bench handling shock as specified in MIL-STD-810, Method 516.1, Procedure V.

b. Landing The FMDM shall be subjected to the landing shock specified in 3.2.5.1h(1).

c. Design The FMDM shall be subjected to design shock as specified in 3.2.5.2h(2) in accordance with MIL-STD-810, Method 516.1, Procedure I.

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d. Crash Safety The FMDM or the chassis of the FMDM with a dummy load simulating the mass and distribution of the remaining elements of the FMDM shall be attached by its normal mounting attachments and subjected to sawtooth shock, as specified in MIL-STD-810, Method 516.1, Procedure III. Crash safety may be verified by analysis.

4.2.4.1.8 Explosive Atmosphere The FMDM shall be subjected to an explosive environmental test in accordance with MIL-STD-810, Method 511, Procedure I, with butane as the fuel. If it can be shown that the FMDM does not contain any arcing or sparking devices, analysis may be used for explosive atmosphere certification. An analysis shall be made to determine that the surface temperature of all internal components exposed to the atmosphere, and the equipment case, will not exceed 352° F during operations.

4.2.4.1.9 Power Tests Tests shall be performed to assure that the FMDM meets performance requirements of Section 3.2.1 and the power consumption requirements of 3.3.3.2.1 with input power meeting the requirements of 3.1.2.1, including both normal and emergency transient conditions, as well as steady-state maximum and minimum limits.

4.2.4.1.10 Lightning Test Lightning tests shall be in accordance with MF0004-002.

4.2.4.1.11 Electromagnetic Compatibility Tests EMC tests which cannot be verified by analysis shall be verified by the minimum susceptibility and omission test developed in accordance with MF0004-002.

4.2.4.1.12 Thermal-Vacuum Tests The FMDM shall be exposed to a vacuum of 10^{-6} torr. The cold plate temperature shall be sequentially cycled between 30° and 125° F for a total of five and one-half cycles.

The temperature rate of change per hour between extremes shall not exceed 240° F or be less than 60° F. The time duration at each temperature extreme shall be sufficient to achieve thermal stabilization plus the time required to conduct a performance test, but shall not be less than 1 hour. The performance test at each high-temperature extreme shall include operation at the maximum heat dissipating mode in accordance with maximum power consumption for the device for a duration consistent with the design capability and sufficient to obtain test data. During the low-temperature extremes, the performance test shall include operation at minimum power consumption for a duration sufficient to verify acceptable performance. Performance tests may start when a pressure of 10^{-5} torr is reached. All circuits shall be monitored during transition between temperature extremes.

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4.2.4.1.13 Operating Life Test On/off cycles and operating time accumulated on a single specimen during other qualification tests may be applied toward these requirements.

a. Cyclic: The FMDM shall be operated for 1000 on/off cycles.

b. Powered: The FMDM shall be operated for 750 hours. The remaining operating hours of Paragraph 3.2.1.1.1 shall be satisfied by analysis.

4.2.4.1.14 Package Qualification Tests Certification of package performance shall be accomplished by analysis whenever possible. When certification cannot be accomplished by analysis, a buyer-approval simulated dummy load shall be installed in its package and both subjected to the applicable FED-STD-101 test to verify conformance to 5.2.3. Development assigned hardware may be used for testing in lieu of a dummy load.

4.2.4.1.15 Thermal Cycle Test The FMDM shall be mounted on a coldplate to simulate usage conditions and subjected to five cycles of the following temperatures.

a. Air Temperature: Plus 165° F
Coldplate Temperature: Refer to Paragraph 4.1.2.1.2

b. Air Temperature: Minus 65° F
Coldplate Temperature: Refer to Paragraph 4.1.2.1.2

The temperature rate of change between extremes shall not exceed 240° F nor be less than 60° F. The time duration at each extreme shall be sufficient to achieve thermal stabilization plus the time required to conduct a performance test, but shall not be less than 1 hour. The performance test at each high-temperature extreme shall include operation at the maximum heat-dissipating mode in accordance with maximum power consumption for the device for a duration consistent with the design capability and sufficient to obtain test data. During the low-temperature extremes, the performance test shall include operation at minimum power consumption for a duration sufficient to verify acceptable performance. All circuits shall be monitored during transition between temperature extremes.

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4.2.4.2 Certification by Analysis The following requirements shall be verified by analysis except where analysis is by similarity.

4.2.4.2.1 Storage/Service Life Compliance with storage/operational life requirements of Section 3 shall be verified by analysis of the applicable documentation and test data.

4.2.4.2.2 Reliability Compliance with the reliability requirements of 3.2.3 shall be verified by analysis and evaluation of design drawings and test data, as applicable.

4.2.4.2.3 Maintainability Compliance with the maintainability requirements of 3.2.4 which cannot be verified by assessment shall be verified by analysis of the engineering data.

4.2.4.2.4 Ozone Compliance with the ozone requirements under 3.2.5 shall be verified by analysis of design drawings and test data.

4.2.4.2.5 Fungus Compliance with the fungus requirements under 3.2.5 shall be verified by analysis of design drawings and test data.

4.2.4.2.6 Materials and Processes Compliance with the materials and processes requirements of 3.3.1.1 which cannot be verified by assessment or test shall be verified by analysis of design drawings and material test data.

4.2.4.2.7 Electromagnetic Compatibility Compliance with the EMC requirements of 3.3.3.1 which cannot be verified by test shall be verified by analysis and design drawings and test data.

4.2.4.2.8 Electrical Design Requirements Compliance with the electrical design requirements under 3.3.3.2 which cannot be verified by test or asessment shall be verified by analysis of design drawings and engineering data.

4.2.4.2.9 Safety Compliance with the safety requirements of 3.3.7 shall be verified by analysis and evaluation of design drawings and test data, as applicable.

4.2.4.2.10 Corrosive Atmosphere All equipment shall be certified for corrosive fluid compatibility when required in accordance with 3.3.1.4. All sensitive material that will be exposed to a corrosive fluid shall be certified for compatibility by analysis based on material test data.

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4.2.4.2.11 Transient Shock Compliance with the transient shock requirement of 3.2.5.1h(2) shall be verified by test or analysis.

4.2.4.2.12 Certification by Other Test Data Test data generated from articles previously certified may be used as a certification method when it can be shown that the article is similar or identical to the article being certified. Features to be considered shall include design, performance, environmental duration and limits, manufacturing process, and quality control. Special effort shall be made to avoid duplication of previous tests from this or similar programs. Where certification by testing is required, data from other than qualificaiton tests may be used to satisfy the requirements under the following conditions:

Predeclaration	The intent to use the test for certification is declared prior to test conduct.
Configuration	Production configuration or approval (where allowed) for differences.
Facilities	Certified.
Inspection	Required.
Test requirement/procedure/ pass-fail criteria	Formally approve by buyer.
Acceptance, functional test pre-, post- and during environment	Required Required (except for nonoperating tests such as packaging).
Documentation	Configuration description, failure reports and test results.

4.2.4.2.13 Mature Hardware (Off-the-Shelf)

a. Evaluate and document equipment capability utilizing a comparison matrix which includes considerations such as configuration, performance and environment versus specified requirements.

b. Where the environmental levels are more stringent than previous qualification levels, analyze or test to verify that the item can withstand the higher level design requirements.

c. For items that require minor modifications or have not been qualified to all environments, only the design modifications for the additional environments need to be certified, if cumulative and interaction effects do not exist. If cumulative and interaction effects do exist, complete qualification testing is required.

4.2.4.2.14 Sand and Dust Compliance with the requirements of Paragraph 3.2.5.2c shall be verified by analysis of design drawings and test data.

4.2.5 Verification Requirements Matrices Reference approved seller's verification plan.

5. PREPARATION FOR DELIVERY

5.1 General Requirements The requirements specified herein govern the preparation for shipment and the transport of the FMDM to all buyer and Government facilities. The method of preservation, packaging and packing utilized for shipment together with necessary special control during transportation shall adequately protect the FMDM from damage or degradation of performance due to the natural and induced environments encountered during transportation and subsequent storage as specified herein.

5.2 Detailed Requirements Packaging, handling, and transportation shall be in accordance with applicable requirements and guidelines of NHB6000.1(A) as supplemented by the following subparagraphs.

5.2.1 Preservation and Packaging Preservation and packaging shall be in accordance with the requirements of Level A of MIL-STD-794.

5.2.2 Packing Packing shall be in accordance with the requirements of Level B of MIL-STD-794.

5.2.3 Design Requirement (Structural) Preservation, packaging, and packing shall be designed to withstand the rough handling, package requirements of MIL-STD-794 as defined in FED-STD-101, (without damage or degradation to the useful life or performance of the contained item, and without damage to the

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preservation, packaging, and packing which would affect their utility) in accordance with the following:

a. Rough Handling

FED-STD-101 Method

5007 Procedure B Free-Fall Flat (Level A)
5007 Procedure E Free-Fall Corner Drop (Level A)
5016 Superimposed Load (with Dunnage) (Level A)
5019 Vibration (Repetitive Shock)
5030 Sinusoidal Vibration

b. Pressure

(1) Transportation: Air 3.28 to 15.23 psia
Ground 9.76 to 15.23 psia

(2) Storage: 12.4 to 15.23 psia

c. Temperature

(1) Transportation: Air minimum; minus 65° F

maximum; plus 150° F for 6 hours
plus 190° F for 1 hour

Ground minimum; minus 40° F

maximum; plus 150° F for 6 hours
plus 190° F for 1 hour

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(2) Storage — Uncontrolled minimum; minus 23° F
maximum; plus 150° F

Controlled nominal; plus 60° to plus 80° F
*minimum; plus 25° F
*maximum; plus 115° F

*Duration 4 hours maximum.

d. Humidity — Air 0 to 100 percent relative
Ground 8 to 100 percent relative

5.2.4 Reusable Containers Where analysis in accordance with NHB6000.1(A) indicates a requirement for reusable containers, maximum practical utilization shall be made of standard off-the-shelf, low-cost metal or plastic containers.

5.2.5 Monitoring Devices MIL-I-26860 humidity indicators shall be installed in the container wall or flexible barrier wall of all Method II (desication) packages for any device that is humidity sensitive.

Utilization of additional instrumentation for monitoring or recording other in transit environments (e.g., shock, vibration, temperature, etc) shall be approved by the buyer prior to implementation.

5.2.6 Temporarily Installed Hardware Identification All temporarily installed devices such as caps, plugs, covers, support bracketry, protective plates, etc, shall be cerise red in color or have attached cerise red colored streamers to ensure that they are easily identified under casual observation. Reusable protective devices shall be labeled REUSABLE ITEM - DO NOT DESTROY - RETAIN FOR REUSE.

5.2.7 Pre-Production Packaging Qualification Tests Testing to verify the functional capability of the package or transport methods/equipment shall be accomplished as required by Section 4 of this specification.

5.2.8 Marking for Shipment Interior and exterior containers shall be marked and labeled in accordance with MIL-STD-129, including precautionary markings necessary to ensure safety of personnel and facilities to ensure safe handling, transport, and storage.

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Packages with reuse capability shall be identified with the words REUSABLE CONTAINER - DO NOT DESTROY - RETAIN FOR REUSE. NASA Critical Item Labels (Form 1368 series) shall be applied in accordance with NHB6000.(1A). Identification information on interior and exterior containers shall be in the following format and shall include:

BUYER CONTROL NUMBER _____

ITEM NAME _____

FSN/NATO STOCK NUMBER _____ (WHEN APPLICABLE)

MANUFACTURER'S TYPE OR PART NUMBER _____

QUANTITY IN PACKAGE _____ TRACEABILITY IDENTIFICATION _____

AGE CONTROL MARKING _____

CLEANING MARKING _____ NOT APPLICABLE

SERIAL NUMBER _____

MANUFACTURER _____

BUYER PURCHASE ORDER NUMBER _____

DATE OF PACKAGING _____

LEVELS OF PACKAGING AND PACKING _____

MANUFACTURER'S PACKAGE PART NUMBER (NOT REQUIRED FOR OFF-THE-SHELF CONTAINERS)

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6. NOTES

6.1 Definitions

6.1.1 Acceptance Tests Inspections and tests to determine that a part, component, subsystem or system is capable of meeting design and performance requirements specified herein.

6.1.2 Assessment A verification method employing inspection and review of design techniques to verify design features not covered by verification test and analysis such as finishes, tolerances, bonding, identification and traceability, safety wiring, warning and service labels, Bill of Materials, etc.

6.1.3 Certification Certification consists of qualification testing, Major Ground Test, and other tests and analyses required to determine that the design hardware from the component through the subsystem level meets requirements.

a. Qualification Test Those tests conducted as part of the certification program to demonstrate that design requirements can be realized under specified conditions.

b. Certification by Analysis Certification by analysis allows the use of appropriate engineering analyses, including simulation, to provide fulfillment of certification objectives. Certification analyses will normally be conducted due to one or both of the following factors.

(1) The inability to simulate specified conditions in an effective ground test.

(2) Qualification testing would not be practical.

Analysis may be used where it can be shown that the article is similar or identical in design, manufacturing processes, and quality control to another article that has been previously certified to equivalent or more stringent criteria.

6.1.4 Development Tests Those tests performed with minimum rigors and controls to verify a design approach.

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6.1.5 Fail Safe The ability to sustain a failure and retain safe operational capability (successfully terminate the mission).

6.1.6 Failure The inability of a system, subsystem, component, or part to perform its required function within specified limits, under specified conditions for a specified duration.

6.1.7 Line Replaceable Unit (LRU) A combination of components, units, parts, assemblies, subassemblies, etc, that are contained in one package, or are so arranged that together the combination is common to one mounting and, in addition, provides a complete function(s) to the larger entity within which it operates.

6.1.8 Shop Relaceable Unit (SRU) An SRU is an integral subassembly of an LRU consisting of units and parts, or a combination of parts so arranged that together the combination is common to one mounting and, in addition, provides a complete function(s) to the larger entity within which it operates.

6.1.9 Scheduled Maintenance The action performed in an attempt to retain an item in a specified condition by providing systematic inspection, detection, and servicing for the prevention of incipient failure.

6.1.10 Operating Cycles The cumulative number of times an item completes a sequence of activation and return to its initial state; e.g., a switched-on/switched-off sequence, a valve-opened/valve-closed sequence, a tank pressurized/depressurized, or dewar cryogenic exposure/drain.

6.1.11 Operating Life The specified operating time/cycles which an item can accrue before replacement or refurbishment without risk of degradation of performance beyond acceptable limits.

6.1.12 Shelf Life That period of time during which an item can remain in storage without having its operability affected. Preventive maintenance, servicing, and replacement of age-sensitive material parts shall be permitted in a scheduled basis during the storage period.

6.1.13 Useful Life The item's total life span, including operating life and storage with normal preventive maintenance, servicing, repair and replacement of parts before item is considered unacceptable for further usage. This life span may be equal to (throw-away), or greater than (repair, refurbishable) the value specified for "operational life."

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6.1.14 Verification The process of planning and implementing a program that determines that the item meets all design, performance, and safety requirements. The verification process includes certification, development testing, acceptance testing, assessment, flight demonstration, preflight checkout, and analysis necessary to support the total verification plan.

6.1.15 Torr The Torr is defined as 1/760 of a standard atmosphere of 1,013,250/760 dynes per square centimeter. This is equivalent to defining the Torr as 1333.22 microbars, and differs by only one part in seven million from the International Standard millimeter of mercury.

6.1.16 Sheltered A warehouse type facility, enclosed, and providing protection against environmental conditions.

6.1.17 Unsheltered An open area and unprotected against environmental conditions.

6.1.18 Built-In-Test Defined as additional circuitry implemented in the basic design of an LRU or system for the purpose of failure detection and/or reporting operational and/or health status of the FMDM. Built-in-test is defined to include: Built-In-Test Equipment (BITE), Self-Test and Test Points.

a. Built-In-Test Equipment (BITE) That circuitry provided to perform continuous monitoring of specific parameters, groups of parameters or functions of the FMDM to provide a Go/No-Go indication. This type of built-in-test capability represents implementation techniques that are autonomous in nature and which provide continuous real-time monitoring but do not interrupt normal operation of the FMDM.

b. Self-Test That circuitry contained in the FMDM which provides the means to simulate operation of an FMDM for the purpose of functional verification. This type of built-in-test capability is nonautonomous in nature in that it may require an external initiation and does interrupt the normal operation of the FMDM.

c. Test Points The measurements of FMDM parameters provided at the electrical interface of the FMDM to enable determination of the relative health or operational status of the individual unit.

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d. Unaugmented Test Defined as a test that does not require the use of the computer in a mode other than the normal operational mission of the data reception/command generation.

e. Probability of Failure Calculation Any acceptable way to calculate the probability of failure detection for an FMDM is:

(1) Failure Rate of Undetected Item Parts Total failure rate of items that affect FMDM ability to meet CEI performance requirements.

For this calculation one can assume the input data to the FMDM is correct and the output faults are due only to the sending FMDM.

6.1.19 Dummy Load For the purpose of shock tests, a dummy load is a duplicate of the shape, size, rigidity, mounting methods, weight, mass distribution and center of gravity of the Qualification Unit. There is no requirement that it be a functioning device.

6.1.20 Failure Criteria Variations of operational and performance characteristics outside of the limits permitted by the detail equipment specification are reason to consider the equipment as having failed. Deterioration and material failure of any part or material which could in any manner prevent the equipment from meeting operation, performance, and reliability requirements during service life shall provide reason to consider the equipment as having failed.

6.1.21 Minimum Cooling The minimum cooling required to prevent the temperature of all critical components within a given unit from exceeding safe levels.

6.1.22 Module A removable plug-in part of an equipment.

6.1.23 RMS Accuracy The RMS error is defined as the square root of the second moment about zero of the error probability density function in the case of a continuous variate. (For a normally distributed error function, with zero mean, the error will be within the RMS value approximately 68 percent of the time. RMS values are one sigma if the mean is zero.) Statistical addition of these errors, if required, shall be accomplished by taking the square root of the sum of the squares of the independent RMS errors.

6.2 Abbreviations and Acronyms Abbreviations and acronyms used in this specification are defined as follows:

A/D	Analog to digital
ATT	Acceptance thermal tests
AVT	Acceptance vibration tests
BITE	Built-in-test equipment
BiØ-L	Biphase level
CDW	Command data word
CG	Center of gravity
CW	Command word
DAC	Digital-to-analog converter
DACBU	Data acquisition control and buffer unit
E	Exempt from traceability
EPC	Error protection code
EPROM	Erasable programmable read-only memory
FMDM	Flexible multiplexer/demultiplexer
GPC	General purpose computer
Hz	Hertz (cycles per second)
I/O	Input/Output
IOP	Input/Output Processor
IPR	Ice point reference
JSC	Johnson Space Center
KΩ	Kilohm
KHz	KiloHertz (kilocycles per second)
LRU	Line-replaceable unit
LSB	Least-significant bit
MDM	Multiplexer/demultiplexer
MHz	MegaHertz (megacycles per second)
MIA	Multiplex interface adapter
MSB	Most-significant bit

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PAM	Pulse amplitude modulated
PC	Pulse code
PCM	Pulse code modulation
PROM	Programmable read-only memory
rms	Root mean square
SCU	Sequence control unit
SD	Space Division
SRU	Shop-replaceable unit
TBD	To be determined
TBS	To be supplied (by seller)
T_L	Lot traceability
T_M	Member traceability
T_S	Serial traceability
µsec	Microseconds
vdc	Volts direct current

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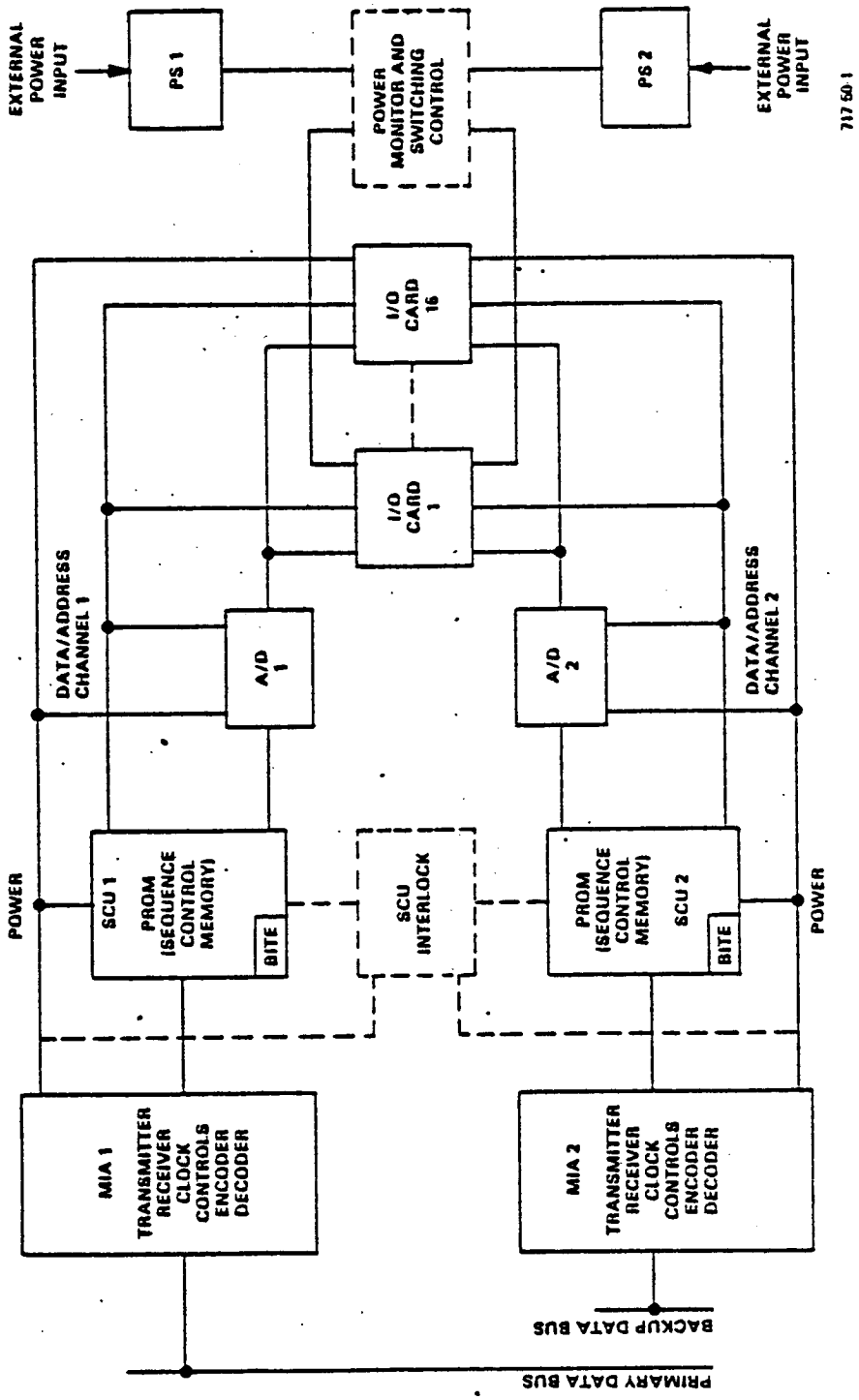


Figure 1
FMDM System Block Diagram (Duplex)

REV LTR

NOTES:
1. ⊕ DENOTES APPROXIMATE CENTER OF GRAVITY.
2. REFERENCE DIMENSIONS FOR INFORMATION ONLY.
3. DIMENSION TOLERANCES: .XX = ± 0.03, .XXX = ± 0.010 UNLESS NOTED OTHERWISE.
4. REMOVE PROTECTIVE COVER PRIOR TO INSTALLATION OR WEIGHT MEASUREMENTS.
5. WITH THE PROTECTIVE COVER REMOVED AND ALL FASTENERS INSTALLED, THE BOTTOM COVER SHALL HAVE A FLATNESS OF .010 AND A 63 SURFACE FINISH.
6. FLATNESS MEASUREMENT SHALL BE MADE WITH THE UNIT MOUNTED TO A SUITABLE PLATE, FLAT WITHIN .002 AFTER UNIT ASSEMBLY. FASTENER TORQUE SHALL BE 40 TO 60 INCH POUNDS. A TOTAL OF 11 POSITIONS SHALL BE INSPECTED ON APPROXIMATELY 3 INCH GRID BY MEANS OF SUITABLE ACCESS HOLES IN PLATE.
7. APPROXIMATE UNIT WEIGHT TBD POUNDS.
8. APPROXIMATE POWER DISSIPATION RANGE TBD
9. UNIT IS DESIGNED FOR COLD PLATE CONDUCTION COOLING THROUGH IT'S MOUNTING SURFACE AND/OR RADIATION COOLING THROUGH IT'S THERMAL RADIATORS.
10. ALL SURFACE FINISHES WILL BE CHOSEN SO AS TO OPTIMIZE CONTROL OF RADIATION HEAT TRANSFER. THE REQUIREMENT FOR A MULTILAYER INSULATION BLANKET IS PER AO.
11. CHASSIS STRUCTURAL AND THERMAL DESIGN INTEGRITY IS ESTABLISHED WHEN THE UNIT IS FULLY POPULATED WITH 12 MODULES AND THE POWER SUPPLY.

CONNECTORS			
REF DES	NASA PART NO.	SPERRY PART NO.	FUNCTION
J1	MLSDE24 35P	4021828-39	SIGNAL
J2	MLSDF24 35PA	4021828-40	SIGNAL
J3	MLSDE24 35SC	4021903-42	SIGNAL
J4	MLSDE24 35SB	4021903-41	SIGNAL
J5	MLSDE16 35P	4021528-19	DATA BUS
J6	MBGH14-05 PN	4021003-18	POWER

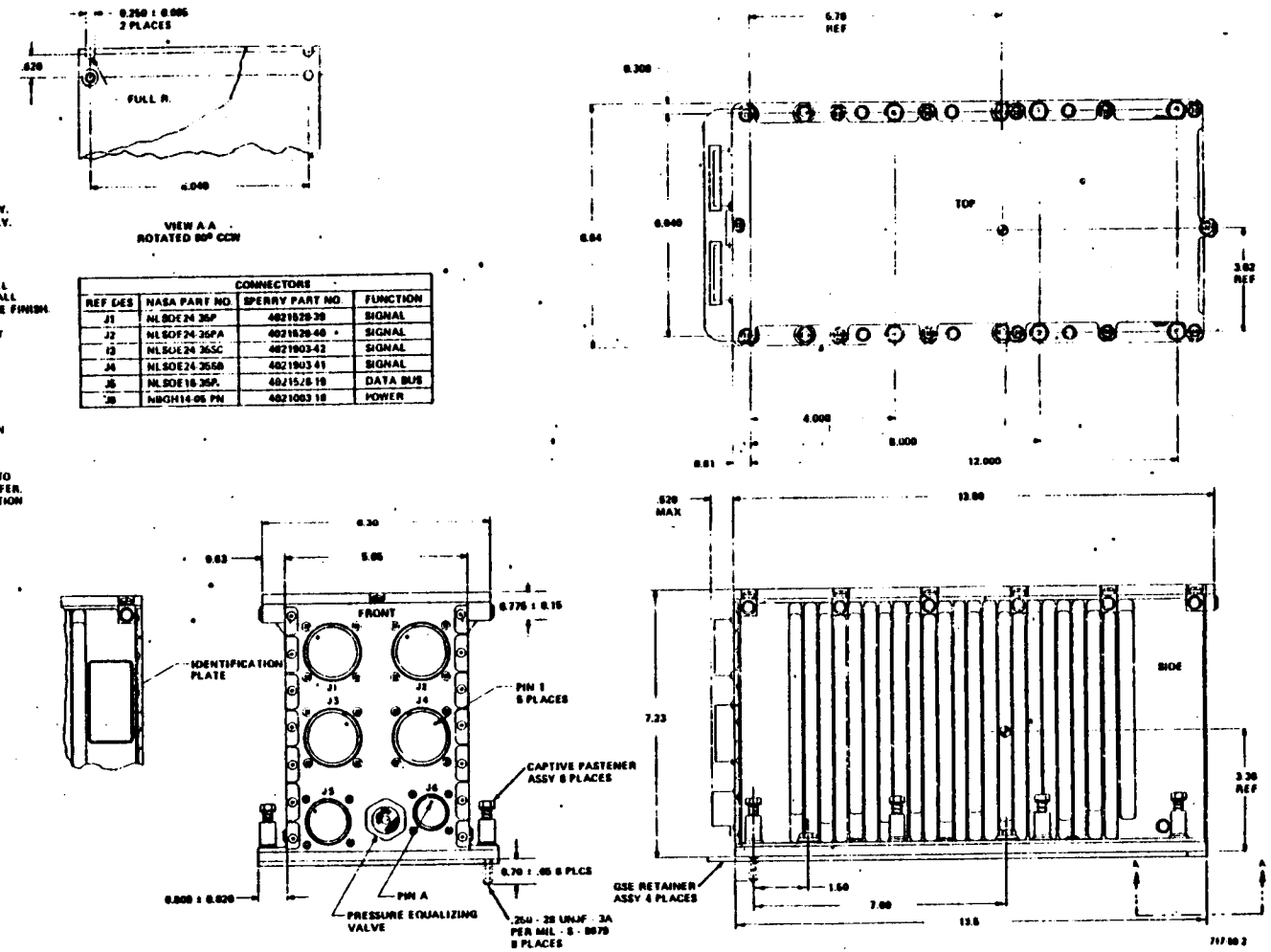
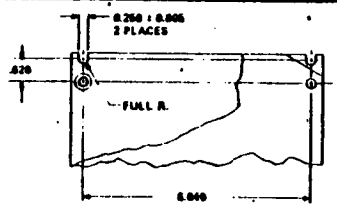


Figure 2
Flexible FMDM LRU Configuration

6200-043 (5-76)

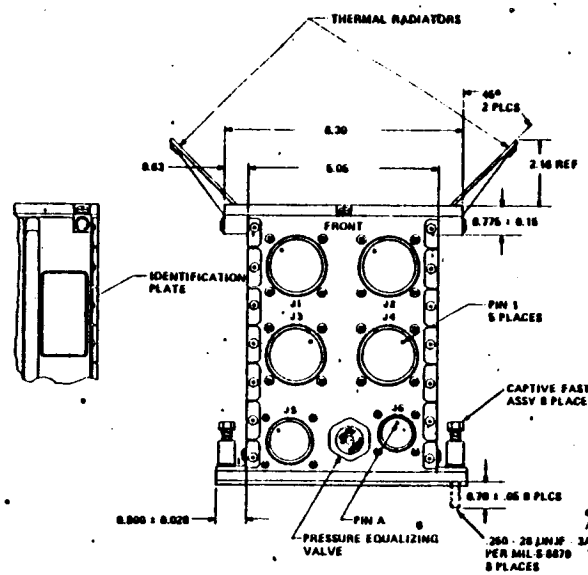
REV LTR

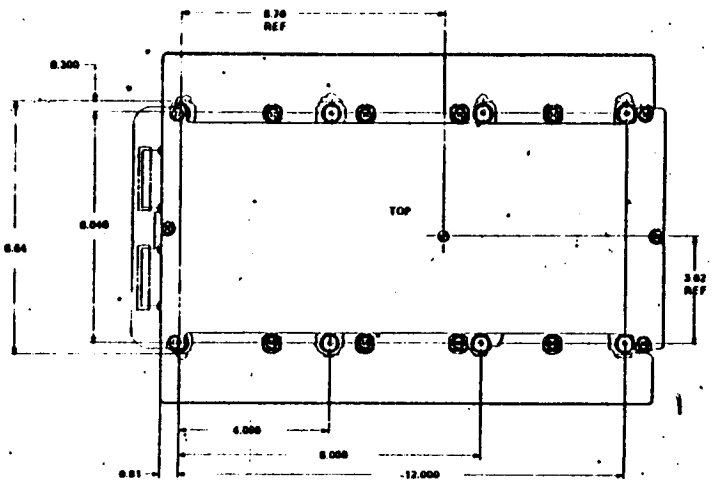
NOTES:
1. ⊕ DENOTES APPROXIMATE CENTER OF GRAVITY.
2. REFERENCE DIMENSIONS FOR INFORMATION ONLY.
3. DIMENSION TOLERANCES: .XX = ± 0.03, .XXX = ± 0.010 UNLESS NOTED OTHERWISE.
4. REMOVE PROTECTIVE COVER PRIOR TO INSTALLATION OR WEIGHT MEASUREMENTS.
5. WITH THE PROTECTIVE COVER REMOVED AND ALL FASTENERS INSTALLED, THE BOTTOM COVER SHALL HAVE A FLATNESS OF .010 AND A 63 SURFACE FINISH.
6. FLATNESS MEASUREMENT SHALL BE MADE WITH THE UNIT MOUNTED TO A SUITABLE PLATE, FLAT WITHIN .002 AFTER UNIT ASSEMBLY. FASTENER TORQUE SHALL BE 40 TO 60 INCH POUNDS. A TOTAL OF 11 POSITIONS SHALL BE INSPECTED ON APPROXIMATELY 3 INCH GRID BY MEANS OF SUITABLE ACCESS HOLES IN PLATE.
7. APPROXIMATE UNIT WEIGHT TBD POUNDS.
8. APPROXIMATE POWER DISSIPATION RANGE TBD
9. UNIT IS DESIGNED FOR COLD PLATE CONDUCTION COOLING THROUGH IT'S MOUNTING SURFACE AND/OR RADIATION COOLING THROUGH IT'S THERMAL RADIATORS.
10. ALL SURFACE FINISHES WILL BE CHOSEN SO AS TO OPTIMIZE CONTROL OF RADIATION HEAT TRANSFER. THE REQUIREMENT FOR A MULTILAYER INSULATION BLANKET IS PER AO.
11. CHASSIS STRUCTURAL AND THERMAL DESIGN INTEGRITY IS ESTABLISHED WHEN THE UNIT IS FULLY POPULATED WITH 12 MODULES AND THE POWER SUPPLY.



VIEW A-A
ROTATED 90° CCW

CONNECTORS			
REF DES	NASA PART NO.	SPERRY PART NO.	FUNCTION
J1	NLSOE24-35P	4021528-39	SIGNAL
J2	NLSOE24-35PA	4021528-40	SIGNAL
J3	NLSOE24-35SC	4021903-42	SIGNAL
J4	NLSOE24-35SB	4021903-41	SIGNAL
J5	NLSOE16-35P	4021528-38	DATA BUS
J6	NBGH14-05 PN	4021003-18	POWER





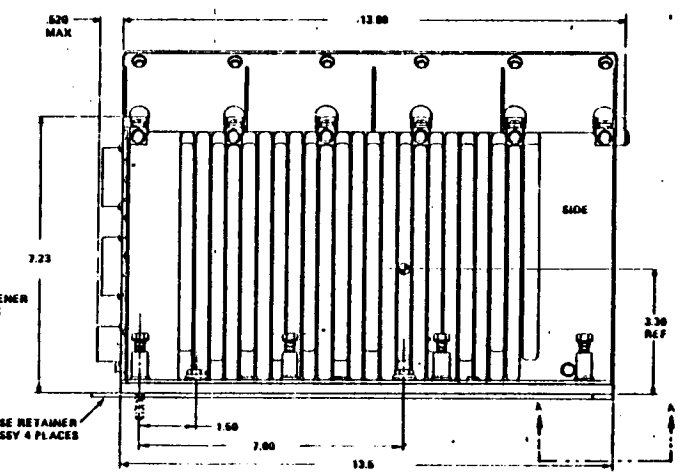


Figure 3
Flexible FMDM LRU Configuration with Radiator

REV LTR

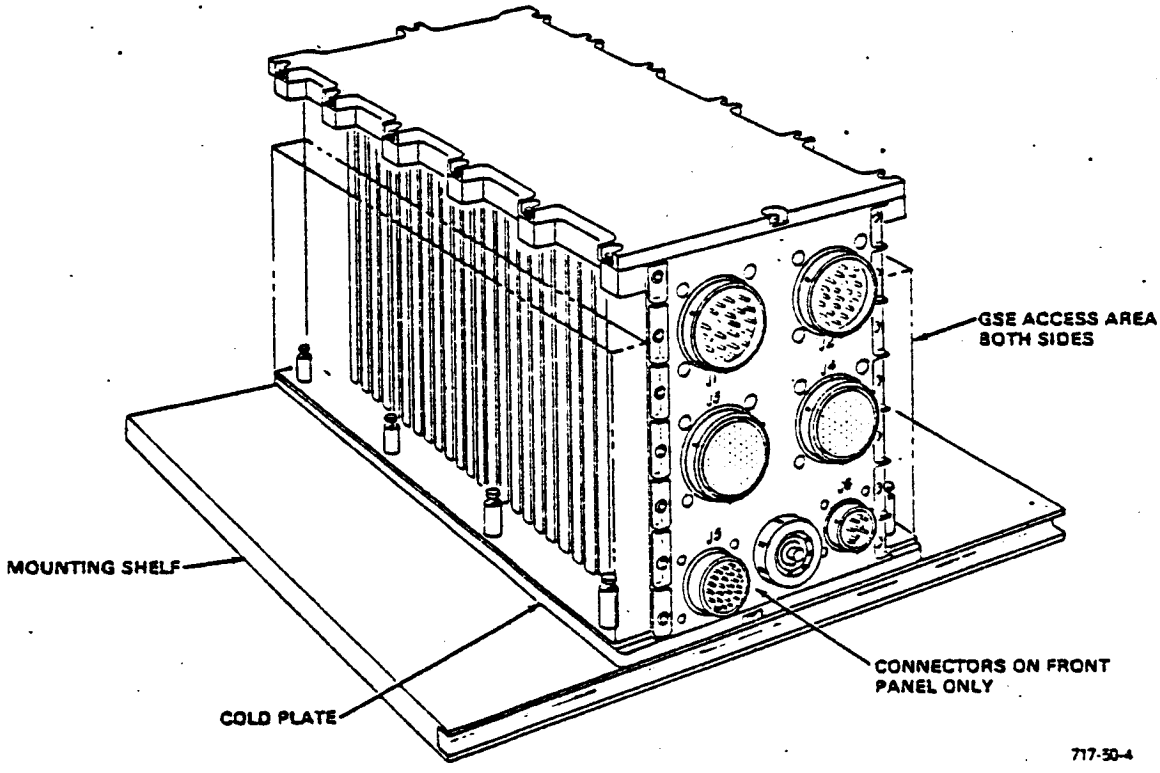


Figure 4
Flexible Simplex Multiplexer/Demultiplexer
LRU Installation on Cold Plate

REV LTR

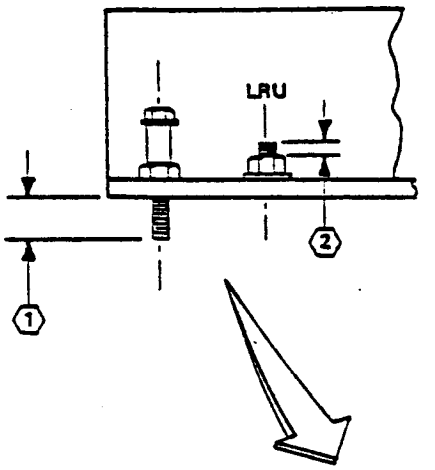
5
10
15
20

T B D

25
30
35
40
45

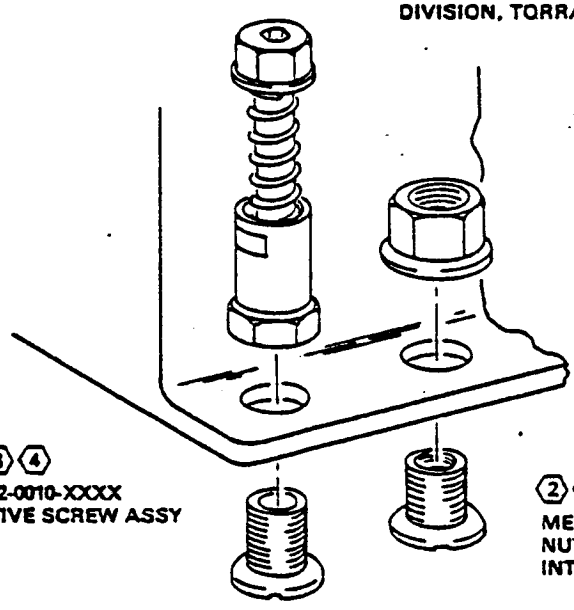
Figure 5
Flexible Simplex Multiplexer/Demultiplexer
LRU Installation with Radiator and
Multilayer Insulation Blanket

REV LTR



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. CAPTIVE BOLT THREADS SHALL PROTRUDE .650 MIN, .750 MAX BELOW THE FLANGE, WHEN FULLY DEPRESSED. PROTRUSION IS TBD WHEN USING THE RADIATOR/ MULTILAYER INSULATION BLANKET CONFIGURATION.
2. NUT RETAINER THREADS SHALL PROTRUDE .030 MIN ABOVE LOCKNUT AFTER INSTALLATION.
3. ALL LRU FASTENER HARDWARE SHALL BE SUPPLIED AND INSTALLED BY VENDOR.
4. FASTENER HARDWARE OBTAINABLE FROM TRIDAIR IND. FASTENER DIVISION, TORRANCE, CAL.



③ MD114-1001-0007
NUT, SELFLOCKING

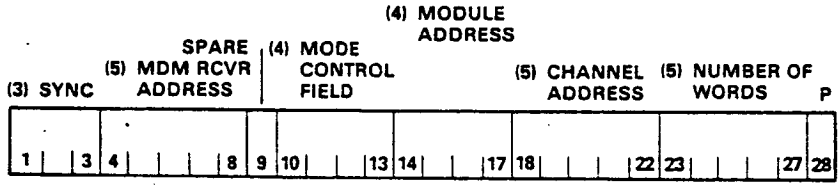
①③④ ME112-0010-XXXX
CAPTIVE SCREW ASSY

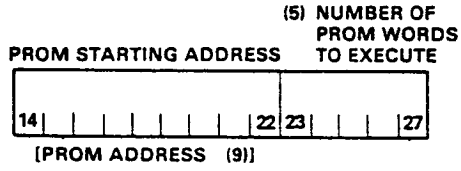
②③④ ME114-0026-XXXX
NUT, RETAINER
INTERNAL THREAD

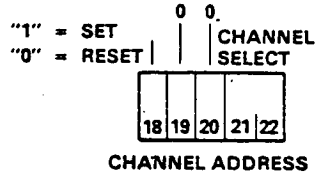
③④ ME114-0025-XXXX
NUT, RETAINER

717-50-5

Figure 6
LRU Fastener Installation







BITS 10	11	12	13	OPERATION
0	0	0	0	SPARE
0	0	0	1	RETURN THE WORD AT THE PROM ADDRESS
0	0	1	0	EXECUTE THE WORD AT THE PROM ADDRESS
0	0	1	1	SPARE
0	1	0	0	COMMAND BITE TEST 1 (SCU)
0	1	0	1	COMMAND BITE TEST 2 (A/D)
0	1	1	0	COMMAND BITE TEST 3 (POWER SUPPLY)
0	1	1	1	COMMAND BITE TEST 4 (10M)
1	0	0	0	PREPARE FMDM TO RECEIVE COMMAND DATA
1	0	0	1	PREPARE FMDM TO TRANSMIT RESPONSE DATA
1	0	1	0	SEND THE BITE STATUS AND RESET THE BITE STATUS REGISTER
1	0	1	1	MASTER RESET; ALL REGISTERS TO LOGIC "0"; ALL OUTPUT SIGNALS TO LOGIC "0"; DC ANALOG OUTPUTS TO 0-VOLTS
1	1	0	0	RETURN THE RECEIVED COMMAND
1	1	0	1	SPARE
1	1	1	0	LOAD BITE STATUS REGISTER (RE: ON-LINE TEST OF BITE STATUS REGISTER)
1	1	1	1	SPARE

717-50-6-R1

Figure 7
Command Word Format

REV LTR

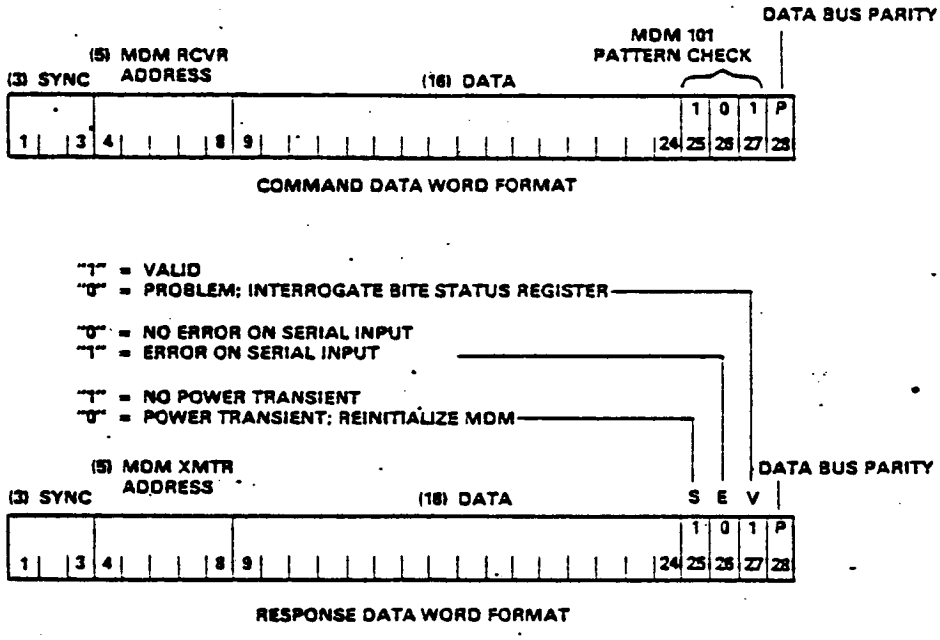


Figure 8
Word Format

REV LTR

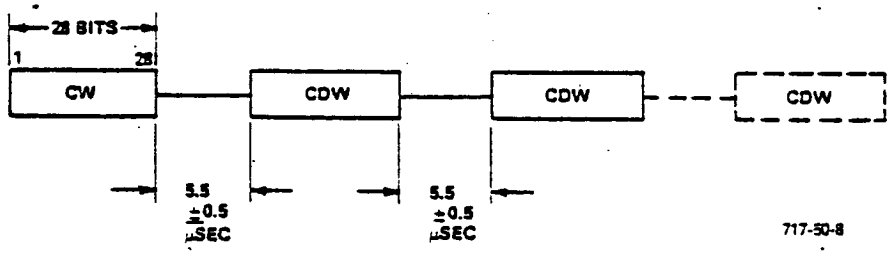


Figure 9
GPC to FMDM Message Sequence

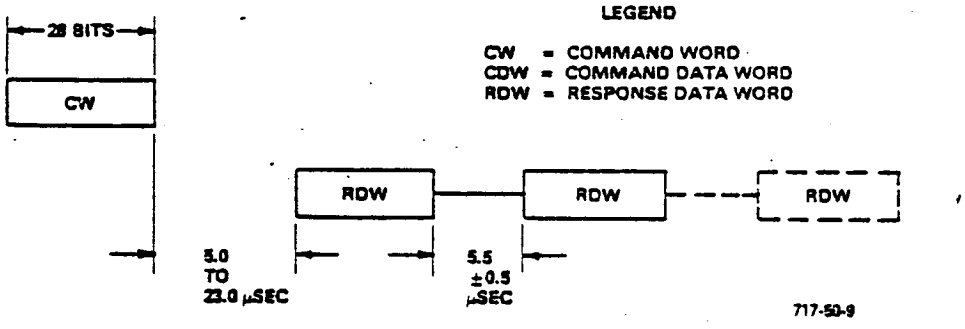


Figure 10
FMDM to GPC Message Sequence

REV LTR

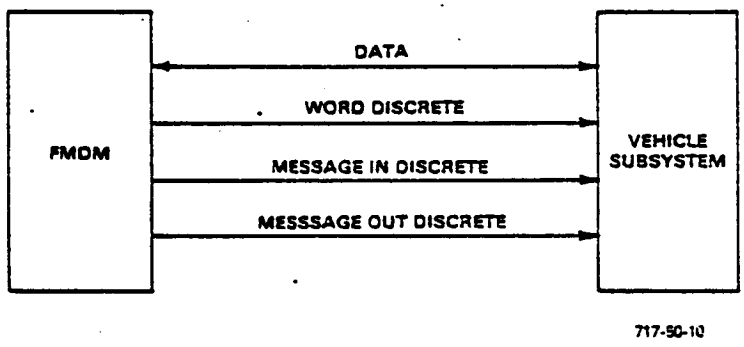
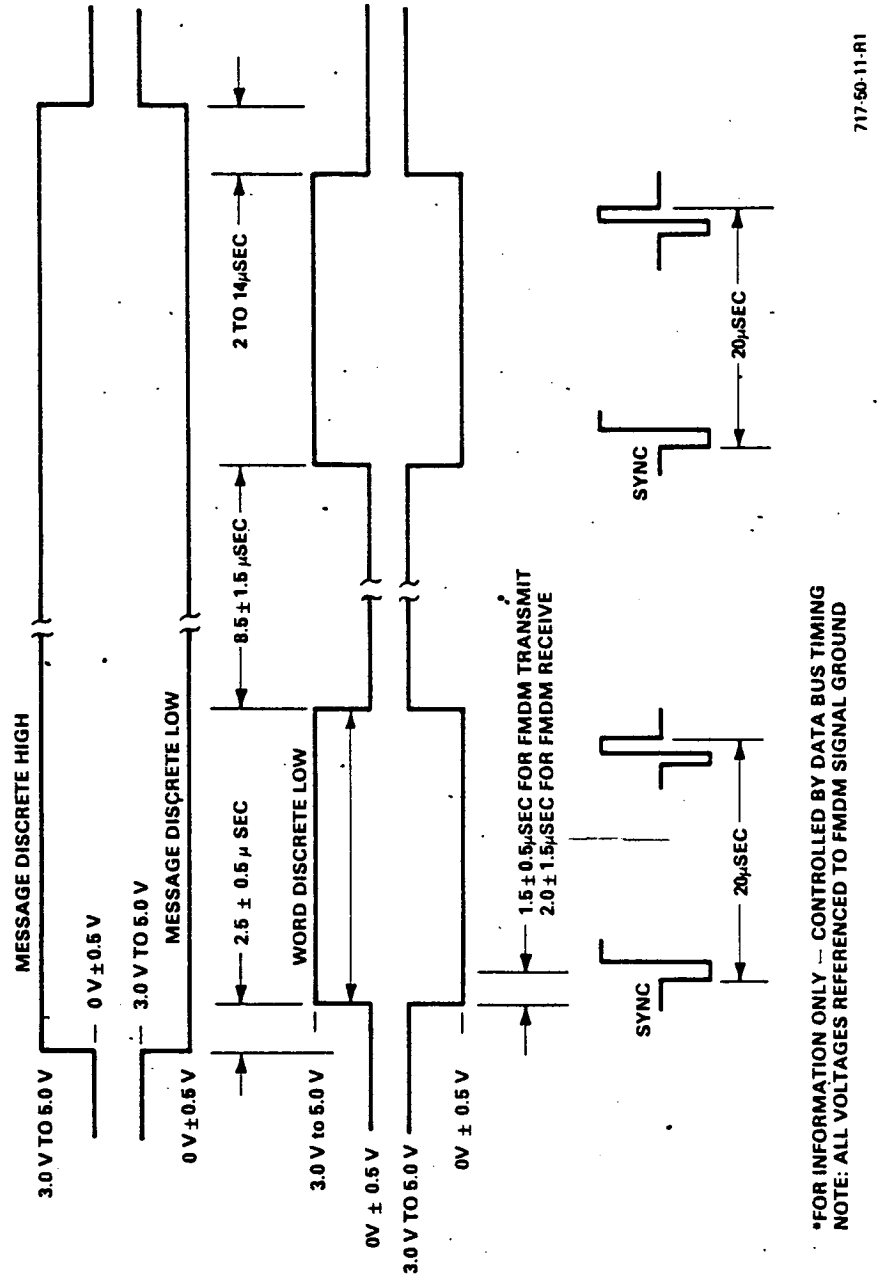


Figure 11
Serial Digit Input/Output Channel Interface

REV LTR



*FOR INFORMATION ONLY — CONTROLLED BY DATA BUS TIMING
NOTE: ALL VOLTAGES REFERENCED TO FMDM SIGNAL GROUND

Figure 12
Serial Channel Data Transfer

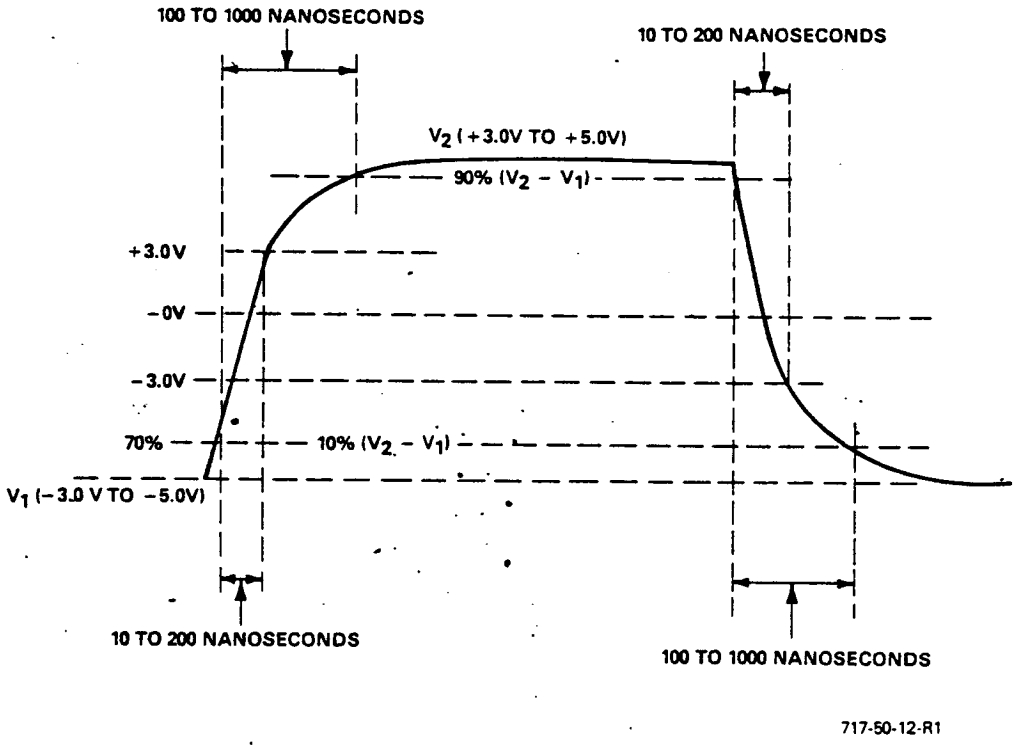


Figure 13
Rise and Fall Times

REV LTR

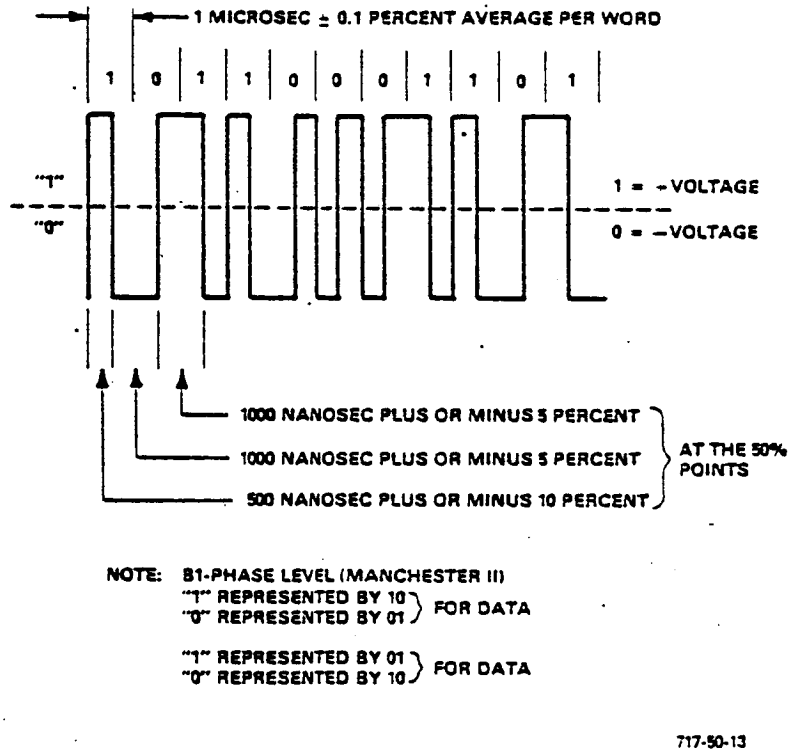


Figure 14
Data Code

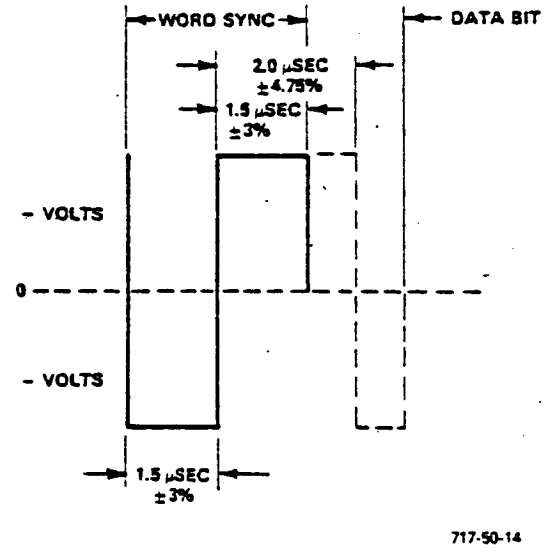


Figure 15
Data Word Sync, Nonvalid Manchester Code

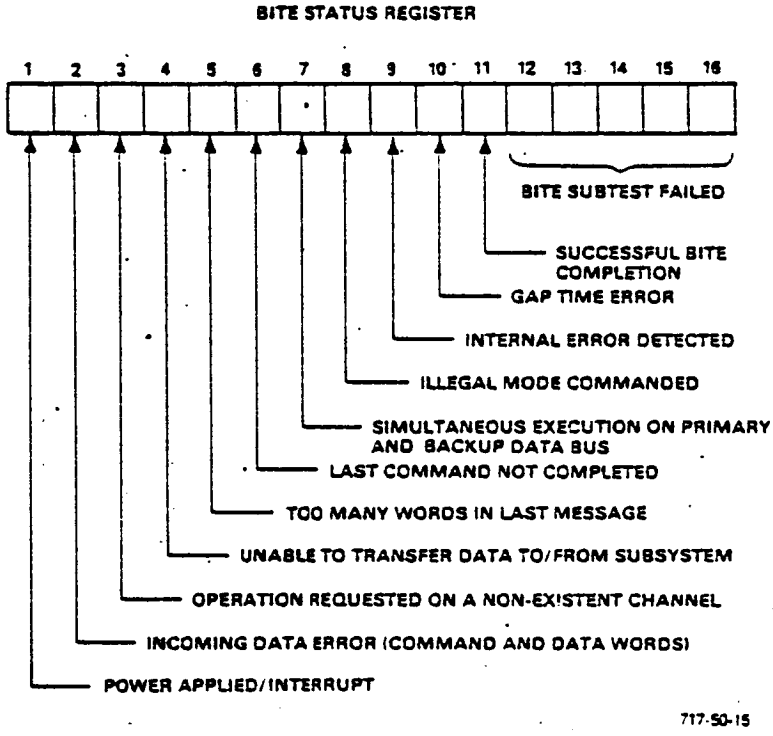


Figure 16
BITE Status Register

APPENDIX A

FLEXIBLE MULTIPLEXER/DEMULTIPLEXER CONFIGURATION

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APPENDIX A

FLEXIBLE MULTIPLEXER/DEMULTIPLEXER CONFIGURATION

FMDM Type	I/O Card No. 0	1	2	3	4	5	6	7
OFT Flight Unit	DI5	DI5	DO5	DO28	DI28	SD	DCIN	DO28
OFT Qual Unit	DI5	SD	DO5	PO28	DI28	DCO	DCIN	DO28

SD - Serial Digital I/O

DCIN - Analog Input Differential

DI28 - Discrete Input High (28 vdc)

DI5 - Discrete Input Low (5 vdc)

DCO - Analog Ouput Differential

DO28 - Discrete Output High (28 vdc)

DO5 - Discrete Output Low (5 vdc)

PO28 - Pulsed Output High (28 volts)

APPENDIX B

INTERFACE PIN/FUNCTION LISTING

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APPENDIX B

INTERFACE PIN/FUNCTION LISTING

SIMPLEX FMDM DATA BUS CONNECTORS

J5 Simplex FMDM

Pin 1	Logic "1"
2	Spare
3	Logic "0"
4	Spare
5	Bit 1 (MSB)
6	Bit 2
7	Bit 3
8	Bit 4
9	Bit 5 (LSB)
10	Spare
11	Data Bus (HI)
12	Data Bus (LO)
13	Spare
14	Spare
15	Spare
16	Program
17	SEQ ADR CSL
18	SEQ ADR 8
19	SEQ ADR 7
20	SEQ ADR 6
21	SEQ ADR 5
22	Spare
23	CLASS GEN OUT
24	CLASS GEN IN
25	SEQ ADR 4
26	SEQ ADR 3
27	SEQ ADR 2
28	SEQ ADR 1
29	SEQ ADR Ø
30	+5V Out
31	+5V In
32	Data I/O Ø
33	Data I/O 1
34	Data I/O 2
35	Data I/O 3

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SIMPLEX FMDM DATA BUS CONNECTORS (cont)

J5 Simplex FMDM

Pin 36	Spare
37	Spare
38	Spare
39	Spare
40	DATA I/O 4
41	DATA I/O 5
42	DATA I/O 6
43	DATA I/O 7
44	Spare
45	-5V Out
46	-5V In
47	Spare
48	Spare
49	Spare
50	Spare
51	Spare
52	Spare
52	Spare
53	Spare
54	+12V Out
55	+12V In

NOTE: Shield tied to connector backshell.

J6 Simplex FMDM

Pin A	+28 vdc
Pin B	DC Return
Pin C	Signal Ground
Pin D	Chassis Ground, if required
Pin E	Shield Ground, if required

NOTE: LO pins will be wired to SMIA pin 2 on prototype and production MIAs.

HI pins will be wired to SMIA pin 18 on prototype and production MIAs.

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SIMPLEX FMDM CONNECTORS AND PINS

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM3	J1	1	CH 1 RET B	CH 1 RET D	CH 3 DATA LO	CH 31 LO	CH 15 LO
		2	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		3	2 RET D	2 RET D		11 LO	5 LO
		4	2 S-10	2 S-10		11 HI	5 HI
		5	2 S-13	2 S-13		13 LO	2 LO
		6	1 RET Spare	1 RET A		13 HI	2 HI
		7	1 S-14	1 S-14		15 LO	4 LO
		8	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
		9	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		10	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		11	2 S-14	2 S-14		10 LO	
		12	2 S-11	2 S-11		10 HI	
		13	2 S-12	2 S-12		12 LO	
		14	1 S-12	1 S-12		15 LO	4 HI
		15	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
		16	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		17	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		18	1 S-8	1 S-8	3 MES OUT LO	29 LO	14 LO
		19	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
		20	2 S-15	2 S-15		9 LO	
		21	2 S-9	2 S-9		9 HI	
		22	2 RET Spare	RET Spare C		12 HI	
		23	1 RET D	RET Spare D		14 LO	
		24	1 S-13	1 S-13		14 HI	
		25	1 S-1	1 S-1	2 MES IN LO	24 LO	13 LO
		26	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		27	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		28	1 S-15	1 S-15	2 WD ENAL HI	26 HI	
		29	1 S-9	1 S-9	3 MES IN LO	28 LO	
		30	1 RET C	1 RET C	3 MES IN HI	28 HI	
		31	Spare	2 RET C		8 LO	
IOM3		32	2 S-8	2 S-8		8 HI	
IOM2		33	1 RET D	RET Spare D		14 LO	
		34	1 S-13	1 S-13		14 HI	
		35	1 S-14	1 S-14		15 LO	4 LO
		36	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
		37	1 S-9	1 S-9	3 MES IN LO	28 LO	
		38	1 RET C	1 RET C	3 MES IN HI	28 HI	
		39	1 RET B	1 RET D	3 DATA LO	31 LO	15 LO
		40	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		41	2 S-15	2 S-15		9 LO	
		42	2 S-9	2 S-9		9 HI	
		43	2 RET D	2 RET D		11 LO	5 LO
		44	2 S-10	2 S-10		11 HI	5 HI
		45	2 S-13	2 S-13		13 LO	2 LO
		46	1 RET Spare	1 RET A		13 HI	2 HI
		47	1 S-12	1 S-12		15 HI	4 HI
		48	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
		49	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
IOM2	J1	50	CH 1 S-0	CH 1 S-0	CH 2 DATA HI	CH 27 HI	CH 11 HI

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SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM2	J1	51	CH 1 S-11	CH 1 S-11	CH 3 WD ENAL LO	CH 30 LO	
		52	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		53	Spare	2 RET C		8 LO	
		54	2 S-5	2 S-5		8 HI	
		55	2 S-14	2 S-14		10 LO	
		56	2 S-11	2 S-11		10 HI	
		57	2 S-12	2 S-12		12 LO	
		58	2 RET Spare	RET Spare C		12 HI	
		59	1 S-1	1 S-1	2 MES IN LO	24 LO	CH 13 LO
		60	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		61	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		62	1 S-15	1 S-15	2 WD ENAL HI	26 HI	
		63	1 S-8	1 S-8	3 MES OUT LO	29 LO	14 LO
IOM2		64	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
IOM1		65	2 S-14	2 S-14		10 LO	
		66	2 S-11	2 S-11		10 HI	
		67	2 S-13	2 S-13		13 LO	2 LO
		68	1 RET Spare	1 RET A		13 HI	2 HI
		69	1 S-14	1 S-14		15 LO	4 LO
		70	1 S-12	1 S-12		15 HI	4 HI
		71	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		72	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		73	1 S-3	1 S-3	3 MES OUT LO	29 LO	14 LO
		74	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
		75	1 RET B	1 RET B	3 DATA LO	31 LO	15 LO
		76	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		77	2 S-15	2 S-15		9 LO	
		78	2 S-9	2 S-9		9 HI	
		79	2 S-12	2 S-12		12 LO	
		80	2 RET Spare	RET Spare C		12 HI	
		81	1 RET D	RET Spare D		14 LO	
		82	1 S-1	1 S-1	2 MES IN LO	24 LO	13 LO
		83	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		84	1 S-15	1 S-15	2 WD ENAL HI	26 HI	
		85	1 S-9	1 S-9	3 MES IN LO	28 LO	
		86	1 RET C	1 RET C	3 MES IN HI	28 HI	
		87	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		88	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		89	Spare	2 RET C		8 LO	
		90	2 S-8	2 S-8		8 HI	
		91	2 RET D	2 RET D		11 LO	5 LO
		92	2 S-10	2 S-10		11 HI	5 HI
		93	1 S-13	1 S-13		14 HI	
		94	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		95	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
IOM1	J1	96	CH 1 S-7	CH 1 S-7	CH 2 MES OUT HI	CH 25 HI	CH 9 HI

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SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOMO	J1	97	CH 1 S-8	CH 1 S-8	CH 3 MES OUT LO	CH 29 LO	CH 14 LO
		98	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
		99	1 RET B	1 RET D	3 DATA LO	31 LO	15 LO
		100	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		101	2 S-12	2 S-12		12 LO	
		102	2 RET Spare	RET Spare C		12 HI	
		103	1 S-14	1 S-14		15 LO	4 LO
		104	1 S-12	1 S-12		15 HI	4 HI
		105	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
		106	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
		107	1 S-9	1 S-9	3 MES IN LO	28 LO	
		108	1 RET C	1 RET C	3 MES IN HI	28 HI	
		109	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		110	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		111	2 RET D	2 RET D		11 LO	5 LO
		112	2 S-10	2 S-10		11 HI	5 HI
		113	1 RET D	RET Spare D		14 LO	
		114	1 S-13	1 S-13		14 HI	
		115	1 S-1	1 S-1	2 MES IN LO	24 LO	13 LO
		116	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		117	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		118	2 S-15	2 S-15		9 LO	
		119	2 S-9	2 S-9		9 HI	
		120	2 S-14	2 S-14		10 LO	
		121	2 S-13	2 S-13		13 LO	2 LO
		122	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		123	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		124	1 S-15	1 S-15	2 WD ENAL HI	26 HI	
		125	Spare	2 REC C		8 LO	
		126	2 S-8	2 S-8		8 HI	
		127	2 S-11	2 S-11		10 HI	
IOMO	J1	128	1 RET Spare	1 RET A		13 HI	2 HI
IOMO	J2	1	0 S-9	0 S-9	1 DATA LO	23 LO	10 LO
		2	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		3	2 S-6	2 S-6		3 LO	
		4	2 S-2	2 S-2		3 HI	
		5	2 S-5	2 S-5		5 LO	
		6	2 RET B	2 RET A		5 HI	
		7	2 RET C	2 RET B		7 LO	
		8	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
		9	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		10	0 S-3	0 S-3	1 WD ENAL HI	22 HI	
		11	2 RET A	RET Spare B		2 LO	1 LO
		12	0 RET Spare	0 RET A		2 HI	1 HI
		13	2 S-7	2 S-7		4 LO	3 LO
		14	2 S-0	2 S-0		7 HI	
		15	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
		16	0 S-14	0 S-14	0 DATA LO	19 LO	12 LO
		17	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		18	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
		19	0 S-4	CH 0 S-4	CH 1 MES OUT HI	21 HI	8 HI
IOMO	J2	20	CH 0 RET D	RET Spare A		CH 1 LO	CH 8 HI

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SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM0	J2	21	CH 0 S-12	CH 0 S-12		CH 1 HI	
		22	2 S-1	2 S-1		4 HI	CH 3 HI
		23	2 S-4	2 S-4		6 LO	
		24	2 S-3	2 S-3		6 HI	
		25	0 S-7	0 S-7	CH 0 MES IN LO	16 LO	7 LO
		26	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		27	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		28	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		29	0 RET A	0 RET C	1 MES IN LO	20 LO	
		30	0 S-5	0 S-5	1 MES IN HI	20 HI	
		31	0 S-11	0 S-11		0 LO	0 LO
IOM0		32	0 S-13	0 S-13		0 HI	0 HI
IOM1		33	2 S-4	2 S-4		6 LO	
		34	2 S-3	2 S-3		6 HI	
		35	2 RET C	2 RET B		7 LO	
		36	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
		37	0 RET A	0 RET C	1 MES IN LO	20 LO	
		38	0 S-5	0 S-5	1 MES IN HI	20 HI	
		39	0 S-9	0 S-9	1 DATA LO	23 LO	10 LO
		40	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		41	0 RET D	RET Spare A		1 LO	
		42	0 S-12	0 S-12		1 HI	
		43	2 S-6	2 S-6		3 LO	
		44	2 S-2	2 S-2		3 HI	
		45	2 S-5	2 S-5		5 LO	
		46	2 RET B	2 RET A		5 HI	
		47	2 S-0	2 S-0		7 HI	
		48	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
		49	0 S-14	0 S-14	0 DATA LO	19 LO	12 LO
		50	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		51	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		52	0 S-3	0 S-3	1 WD ENAL HI	22 HI	
		53	0 S-11	0 S-11		0 LO	0 LO
		54	0 S-13	0 S-13		0 HI	0 HI
		55	2 RET A	RET Spare B		2 LO	1 LO
		56	0 RET Spare	0 Ret A		2 HI	1 HI
		57	2 S-7	2 S-7		4 LO	3 LO
		58	2 S-1	2 S-1		4 HI	3 HI
		59	0 S-7	0 S-7	0 MES IN LO	16 LO	7 LO
		60	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		61	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		62	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		63	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
IOM1	J2	64	CH 0 S-4	CH 0 S-4	CH 1 MES OUT HI	CH 21 HI	CH 8 HI

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SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM2	J2	65	CH 2 RET A	CH RET Spare B		CH 2 LO	CH 1 LO
		66	0 RET Spare	0 RET A		2 HI	1 HI
		67	2 S-5	2 S-5		5 LO	
		68	2 RET B	2 RET A		5 HI	
		69	2 RET C	2 RET B		7 LO	
		70	2 S-0	2 S-0		7 HI	
		71	0 S-14	0 S-14	CH 0 DATA LO	19 LO	12 LO
		72	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		73	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
		74	0 S-4	0 S-4	1 MES OUT HI	21 HI	8 HI
		75	0 S-9	0 S-9	1 DATA LO	23 LO	10 LO
		76	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		77	0 RET D	RET Spare A		1 LO	
		78	0 S-12	0 S-12		1 HI	
		79	2 S-7	2 S-7		4 LO	3 LO
		80	2 S-1	2 S-1		4 HI	3 HI
		81	2 S-4	2 S-4		6 LO	
		82	0 S-7	0 S-7	0 MES IN LO	16 LO	7 LO
		83	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		84	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		85	0 RET A	0 RET C	1 MES IN LO	20 LO	
		86	0 S-5	0 S-5	1 MES IN HI	20 HI	
		87	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		88	0 S-3	0 S-3	1 WD ENAL HI	22 HI	
		89	0 S-11	0 S-11		0 LO	0 LO
		90	0 S-13	0 S-13		0 HI	0 HI
		91	2 S-6	2 S-6		3 LO	
		92	2 S-2	2 S-2		3 HI	
		93	2 S-3	2 S-3		6 HI	
		94	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		95	0 S-6	0 S-6	0 MES IN LO	17 LO	6 LO
IOM2		96	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
IOM3		97	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
		98	0 S-4	0 S-4	1 MES OUT HI	21 HI	8 HI
		99	0 S-9	0 S-9	1 DATA LO	23 LO	10 LO
		100	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		101	2 S-7	2 S-7		4 LO	3 LO
		102	2 S-1	2 S-1		4 HI	3 HI
		103	2 RET C	2 RET B		7 LO	
		104	2 S-0	2 S-0		7 HI	
		105	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
		106	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
		107	0 RET A	0 RET C	1 MES IN LO	20 LO	
		108	0 S-5	0 S-5	1 MES IN HI	20 HI	
		109	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		110	0 S-3	0 S-3	1 WD ENAL HI	22 HI	
		111	2 S-6	2 S-6		3 LO	
		112	2 S-2	2 S-2		3 HI	
		113	2 S-4	2 S-4		6 LO	
		114	2 S-3	2 S-3		6 HI	
IOM3	J2	115	CH 0 S-7	CH 0 S-7	CH 0 MES IN LO	CH 16 LO	CH 7 LO

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SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM3	J2	116	CH 0 S-14	CH 0 S-14	CH 0 DATA LO	CH 19 LO	CH 12 LO
		117	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		118	0 RET D	RET Spare A		1 LO	
		119	0 S-12	0 S-12		1 HI	
		120	2 RET A	RET Spare B		2 LO	1 LO
		121	2 S-5	2 S-5		5 LO	
		122	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		123	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		124	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		125	0 S-11	0 S-11		0 LO	0 LO
		126	0 S-13	0 S-13		0 HI	0 HI
		127	0 RET Spare	0 RET A		2 HI	1 HI
IOM3	J2	128	2 RET B	2 RET A		5 HI	
IOM4	J3	1	1 RET B	1 RET D	3 DATA LO	31 LO	15 LO
		2	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		3	2 RET D	2 RET D		11 LO	5 LO
		4	2 S-10	2 S-10		11 HI	5 HI
		5	2 S-13	2 S-13		13 LO	2 LO
		6	1 RET Spare	1 RET A		13 HI	2 HI
		7	1 S-14	1 S-14		15 LO	4 LO
		8	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
		9	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		10	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		11	2 S-14	2 S-14		10 LO	
		12	2 S-11	2 S-11		10 HI	
		13	2 S-12	2 S-12		12 LO	
		14	1 S-12	1 S-12		15 LO	4 HI
		15	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
		16	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		17	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		18	1 S-3	1 S-3	3 MES OUT LO	29 LO	14 LO
		19	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
		20	2 S-15	2 S-15		9 LO	
		21	2 S-9	2 S-9		9 HI	
		22	2 RET Spare	RET Spare C		12 HI	
		23	1 RET D	RET Spare D		14 LO	
		24	1 S-13	1 S-13		14 HI	
		25	1 S-1	1 S-1	2 MES IN LO	24 LO	13 LO
		26	1 S-6	1 S-6	2 MES IN HI	24 HI	CH 13 HI
		27	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		28	1 S-15	1 S-15	2 WD ENAL HI	26 HI	
		29	1 S-9	1 S-9	3 MES IN LO	28 LO	
		30	1 RET C	1 RET C	CH 3 MES IN HI	28 HI	
		31	Spare	2 RET C		8 LO	
IOM4	J3	32	CH 2 S-8	CH 2 S-8		CH 8 HI	

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SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM5	J3	33	CH 1 RET D	CH RET Spare D		CH 14 LO	
		34	1 S-13	1 S-13		14 HI	
		35	1 S-14	1 S-14		15 LO	CH 4 LO
		36	1 S-5	1 S-5	CH 2 MES OUT LO	25 LO	9 LO
		37	1 S-9	1 S-9	3 MES IN LO	28 LO	
		38	1 RET C	1 RET C	3 MES IN HI	28 HI	
		39	1 RET B	1 RET D	3 DATA LO	31 LO	15 LO
		40	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		41	2 S-15	2 S-15		9 LO	
		42	2 S-9	2 S-9		9 HI	
		43	2 RET D	2 RET D		11 LO	5 LO
		44	2 S-10	2 S-10		11 HI	5 HI
		45	2 S-13	2 S-13		13 LO	2 LO
		46	1 RET Spare	1 RET A		13 HI	2 HI
		47	1 S-12	1 S-12		15 HI	4 HI
		48	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
		49	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		50	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		51	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		52	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		53	Spare	2 RET C		8 LO	
		54	2 S-8	2 S-8		8 HI	
		55	2 S-14	2 S-14		10 LO	
		56	2 S-11	2 S-11		10 HI	
		57	2 S-12	2 S-12		12 LO	
		58	2 RET Spare	RET Spare C		12 HI	
		59	1 S-1	1 S-1	2 MES IN LO	24 LO	13 LO
		60	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		61	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		62	1 S-15	1 S-15	2 WD ENAL HI	26 HI	
		63	1 S-8	1 S-8	3 MES OUT LO	29 LO	14 LO
IOM5		64	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
IOM6		65	2 S-14	2 S-14		10 LO	
		66	2 S-11	2 S-11		10 HI	
		67	2 S-13	2 S-13		13 LO	2 LO
		68	1 RET Spare	1 RET A		13 HI	2 HI
		69	1 S-14	1 S-14		15 LO	4 LO
		70	1 S-12	1 S-12		15 HI	4 HI
		71	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		72	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		73	1 S-8	1 S-8	3 MES OUT LO	29 LO	14 LO
		74	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
		75	1 RET B	1 RET D	3 DATA LO	31 LO	15 LO
		76	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		77	2 S-15	2 S-15		9 LO	
		78	2 S-9	2 S-9		9 HI	
		79	2 S-12	2 S-12		12 LO	
		80	2 RET Spare	RET Spare C		12 HI	
		81	1 RET D	RET Spare D		14 LO	
		82	1 S-1	1 S-1	2 MES IN LO	24 LO	CH 13 LO
		83	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
IOM6	J3	84	CH 1 S-15	CH 1 S-15	CH 2 WD ENAL HI	CH 26 HI	

REV LTR

SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM6	J3	85	CH 1 S-9	CH 1 S-9	CH 3 MES IN LO	CH 28 LO	
		86	1 RET C	1 RET C	3 MES IN HI	28 HI	
		87	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		88	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		89	Spare	2 RET C		8 LO	
		90	2 S-8	2 S-8		8 HI	
		91	2 RET D	2 RET D		11 LO	CH 5 LO
		92	2 S-10	2 S-10		11 HI	5 HI
		93	1 S-13	1 S-13		14 HI	
		94	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		95	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
IOM6		96	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
IOM7		97	1 S-5	1 S-5	3 MES OUT LO	29 LO	14 LO
		98	1 S-2	1 S-2	3 MES OUT HI	29 HI	14 HI
		99	1 RET B	1 RET D	3 DATA LO	31 LO	15 LO
		100	1 S-4	1 S-4	3 DATA HI	31 HI	15 HI
		101	2 S-12	2 S-12		12 LO	
		102	2 RET Spare	RET Spare C		12 HI	
		103	1 S-14	1 S-14		15 LO	4 LO
		104	1 S-12	1 S-12		15 HI	4 HI
		105	1 S-5	1 S-5	2 MES OUT LO	25 LO	9 LO
		106	1 S-7	1 S-7	2 MES OUT HI	25 HI	9 HI
		107	1 S-9	1 S-9	3 MES IN LO	28 LO	
		108	1 RET C	1 RET C	3 MES IN HI	28 HI	
		109	1 S-11	1 S-11	3 WD ENAL LO	30 LO	
		110	1 S-3	1 S-3	3 WD ENAL HI	30 HI	
		111	2 RET D	2 RET D		11 LO	5 LO
		112	2 S-10	2 S-10		11 HI	5 HI
		113	1 RET D	RET Spare D		14 LO	
		114	1 S-13	1 S-13		14 HI	
		115	1 S-1	1 S-1	2 MES IN LO	24 LO	13 LO
		116	1 S-10	1 S-10	2 DATA LO	27 LO	11 LO
		117	1 S-0	1 S-0	2 DATA HI	27 HI	11 HI
		118	2 S-15	2 S-15		9 LO	
		119	2 S-9	2 S-9		9 HI	
		120	2 S-14	2 S-14		10 LO	
		121	2 S-13	2 S-13		13 LO	2 LO
		122	1 S-6	1 S-6	2 MES IN HI	24 HI	13 HI
		123	1 RET A	1 RET B	2 WD ENAL LO	26 LO	
		124	1 S-15	1 S-15	CH 2 WD ENAL HI	26 HI	
		125	Spare	2 RET C		8 LO	
		126	2 S-8	2 S-8		8 HI	
		127	2 S-11	2 S-11		10 HI	
IOM7	J3	128	CH 1 RET Spare	CH 1 RET A		CH 13 HI	CH 2 HI

REV LTR

SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM7	J4	1	CH 0 S-9	CH 0 S-9	CH 1 DATA LO	CH 23 LO	CH 10 LO
		2	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		3	2 S-6	2 S-6		3 LO	
		4	2 S-2	2 S-2		3 HI	
		5	2 S-5	2 S-5		5 LO	
		6	2 RET B	2 RET A		5 HI	
		7	2 RET C	2 RET B		7 LO	
		8	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
		9	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		10	0 S-3	0 S-3	1 WD ENAL HI	22 HI	
		11	2 RET A	RET Spare B		2 LO	1 LO
		12	0 RET Spare	0 RET A		2 HI	1 HI
		13	2 S-7	2 S-7		4 LO	3 LO
		14	2 S-0	2 S-0		7 HI	
		15	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
		16	0 S-14	0 S-14	0 DATA LO	19 LO	12 LO
		17	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		18	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
		19	0 S-4	0 S-4	1 MES OUT HI	21 HI	8 HI
		20	0 RET D	RET Spare A		1 LO	
		21	0 S-12	0 S-12		1 HI	
		22	2 S-1	2 S-1		4 HI	3 HI
		23	2 S-4	2 S-4		6 LO	
		24	2 S-3	2 S-3		6 HI	
		25	0 S-7	0 S-7	0 MES IN LO	16 LO	7 LO
		26	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		27	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		28	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		29	0 RET A	0 RET C	1 MES IN LO	20 LO	
		30	0 S-5	0 S-5	1 MES IN HI	20 HI	
		31	0 S-11	0 S-11		0 LO	0 LO
IOM7		32	0 S-13	0 S-13		0 HI	0 HI
IOM6		33	2 S-4	2 S-4		6 LO	
		34	2 S-3	2 S-3		6 HI	
		35	2 RET C	2 RET B		7 LO	
		36	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
		37	0 RET A	0 RET C	1 MES IN LO	20 LO	
		38	0 S-5	0 S-5	1 MES IN HI	20 HI	
		39	0 S-9	0 S-9	1 DATA LO	23 LO	10 LO
		40	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		41	0 RET D	RET Spare A		1 LO	
		42	0 S-12	0 S-12		1 HI	
		43	2 S-6	2 S-6		3 LO	
		44	2 S-2	2 S-2		3 HI	
		45	2 S-5	2 S-5		5 LO	
		46	2 RET B	2 RET A		5 HI	
		47	2 S-0	2 S-0		7 HI	
		48	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
		49	0 S-14	0 S-14	0 DATA LO	19 LO	12 LO
		50	0 S-2	0 S-2	0 DATA HI	19 HI	CH 12 HI
IOM6	J4	51	CH 0 S-10	CH S-10	CH 1 WD ENAL LO	CH 22 LO	

REV LTR

SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM6	J4	52	CH 0 S-3	CH 0 S-3	CH 1 WD ENAL HI	CH 22 HI	
		53	0 S-11	0 S-11		0 LO	CH 0 LO
		54	0 S-13	0 S-13		0 HI	0 HI
		55	2 RET A	RET Spare B		2 LO	1 LO
		56	0 RET Spare	0 RET A		2 HI	1 HI
		57	2 S-7	2 S-7		4 LO	3 LO
		58	2 S-1	2 S-1		4 HI	3 HI
		59	0 S-7	0 S-7	0 MES IN LO	16 LO	7 LO
		60	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		61	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		62	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		63	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
IOM6		64	0 S-4	0 S-4	1 MES OUT HI	21 HI	8 HI
IOM5		65	2 RET A	RET Spare B		2 LO	1 LO
		66	0 RET Spare	0 RET A		2 HI	1 HI
		67	2 S-5	2 S-5		5 LO	
		68	2 RET B	2 RET A		5 HI	
		69	2 RET C	2 RET B		7 LO	
		70	2 S-0	2 S-0		7 HI	
		71	0 S-14	0 S-14	0 DATA LO	19 LO	12 LO
		72	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		73	0 S-8	0 S-8	1 MES OUT LO	21 LO	8 LO
		74	0 S-4	0 S-4	1 MES OUT HI	21 HI	8 HI
		75	0 S-9	0 S-9	1 DATA LO	23 LO	10 LO
		76	0 RET C	0 RET D	1 DATA HI	23 HI	10 HI
		77	0 RET D	RET Spare A		1 LO	
		78	0 S-12	0 S-12		1 HI	
		79	2 S-7	2 S-7		4 LO	3 LO
		80	2 S-1	2 S-1		4 HI	3 HI
		81	2 S-4	2 S-4		6 LO	
		82	0 S-7	0 S-7	0 MES IN LO	16 LO	7 LO
		83	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		84	0 RET B	0 RET B	0 WD ENAL HI	18 HI	
		85	0 RET A	0 RET C	1 MES IN LO	20 LO	
		86	0 S-5	0 S-5	1 MES IN HI	20 HI	
		87	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		88	0 S-3	0 S-3	1 WD EANL HI	22 HI	
		89	0 S-11	0 S-11		0 LO	0 LO
		90	0 S-13	0 S-13		0 HI	0 HI
		91	2 S-6	2 S-6		3 LO	
		92	2 S-2	2 S-2		3 HI	
		93	2 S-3	2 S-3		6 HI	
		94	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		95	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
IOM5	J4	96	CH 0 S-1	CH 0 S-1	CH 0 MES OUT HI	CH 17 HI	CH 6 HI

REV LTR

SIMPLEX FMDM CONNECTORS AND PINS (cont)

Card	Conn	Pin	Input Discretes	Output Discretes	Serial	DCIN	DCO
IOM4	J4	97	CH 0 S-8	CH 0 S-8	CH 1 MES OUT LO	CH 21 LO	CH 8 LO
		98	0 S-4	0 S-4	1 MES OUT HI	21 HI	8 HI
		99	0 S-9	0 S-9	1 DATA LO	23 LO	
		100	0 RET C	0 DET D	1 DATA HI	23 HI	10 HI
		101	2 S-7	2 S-7		4 LO	3 LO
		102	2 S-1	2 S-1		4 HI	3 HI
		103	2 RET C	2 RET B		7 LO	
		104	2 S-0	2 S-0		7 HI	
		105	0 S-6	0 S-6	0 MES OUT LO	17 LO	6 LO
		106	0 S-1	0 S-1	0 MES OUT HI	17 HI	6 HI
		107	0 RET A	0 RET C	1 MES IN LO	20 LO	
		108	0 S-5	0 S-5	1 MES IN HI	20 HI	
		109	0 S-10	0 S-10	1 WD ENAL LO	22 LO	
		110	0 S-3	0 S-3	1 WD ENAL HI	22 HI	
		111	2 S-6	2 S-6		3 LO	
		112	2 S-2	2 S-2		3 HI	
		113	2 S-4	2 S-4		6 LO	
		114	2 S-3	2 S-3		6 HI	
		115	0 S-7	0 S-7	0 MES IN LO	16 LO	7 LO
		116	0 S-14	0 S-14	0 DATA LO	19 LO	12 LO
		117	0 S-2	0 S-2	0 DATA HI	19 HI	12 HI
		118	0 RET D	RET Spare A		1 LO	
		119	0 S-12	0 S-12		1 HI	
		120	2 RET A	RET Spare B		2 LO	1 LO
		121	2 S-5	2 S-5		5 LO	
		122	0 S-0	0 S-0	0 MES IN HI	16 HI	7 HI
		123	0 S-15	0 S-15	0 WD ENAL LO	18 LO	
		124	0 RET B	0 RET B	CH 0 WD ENAL HI	18 HI	
		125	0 S-11	0 S-11		0 LO	0 LO
		126	0 S-13	0 S-13		0 HI	0 HI
		127	0 RET Spare	0 RET A		2 HI	CH 1 HI
IOM4	J4	128	CH 2 RET B	CH 2 RET A		CH 5 HI	